An FVF-Based Gm-Enhanced fully balanced Preamplifier

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Abstract
A High-gain, fully balanced preamplifier is presented. The proposed structure advantages flipped voltage follower scheme to achieve a compact current conveyor with very low input impedance. The presented current conveyor then is used as a core element to realize a high-gain, gm-enhanced trans-conductance amplifier. The presented amplifier is suitable for application as a preamplifier. The high gain of amplifier makes it very suitable to be configured in a feedback form to deliver a high-precision predefined or programmable amplification gain. The proposed structure draws a very low power of 150nW from a 0.6V supply voltage.
The Spectre Post-layout simulations with TSMC 180nm CMOS technology have been performed. The proposed amplifier exhibits an open-loop DC gain of 141.5dB and 3-dB frequency bandwidth of 2.4kHz at 60dB closed-loop configuration. The load capacitance is set to be 5pF. The proposed structure also delivers high CMRR and PSRR values of 148.3dB and 153.7dB, respectively.

Keywords
FVF, OTA, Low power, Low voltage, CCII, Preamplifier.

1. Introduction

Nowadays, technology downscaling, which is driven by digital CMOS technology and accompanied by increasing demand for emerging low-power (LP), low-voltage (LV), and battery-operated devices has enforced the analog designs with some serious challenges [1, 2]. Neighboring with digital systems, the analog circuits must be capable of operating in very reduced supply voltages, the condition which normally is the worst for the performance of analog blocks.
A serious problem faced by analog designers is that as the technology and accordingly the supply voltage is scaled down, the transistor threshold (V_{th}) and saturation ($V_{ds,sat}$) voltages are not scaled down in the same percentage, which causes degradation of transistor parameters [3]. Some of the parameters that majorly affected are voltage dynamic range (DR), intrinsic voltage gain (VG), trans-conductance (Gm), frequency bandwidth (BW), and noise performance (NP). The direct result of degradation of transistor parameters is performance and design validity reduction of circuits. Unfortunately, most of the conventional designs and circuit structures fail to operate appropriately in these stringent conditions. This necessitates revising the old structures and performing some modifications with the intention of making them suitable to operate in a low-voltage regime. Novel structures are also very welcome. Some efforts in this regard can be found in [4-9].
Operational trans-conductance amplifier (OTA) is one of the most important analog blocks that has a vast application in LP and LV designs. Though, numerous OTA structures have been introduced by the design community to address the needs of low-voltage design areas. Nevertheless, the design of OTA in LV regime is rather challenging. Routinely cascode structure should be avoided as much as possible. Meaning some well-accepted structure such as folded cascode (FC) OTAs which has shown proven performance (especially in communication circuits) should be discarded or at least majorly revised in design. One general solution may be revising the designs to operate in subthreshold regime. This relaxes most of the problems associated with LV design, yet bring some limits foreground, such as limited speed performance. Among other well-stablished low voltage design techniques are using floating gate [10, 11] and bulk-driven [6, 12, 13] transistors in circuit design. These methods are very effective in reducing the required supply voltage. However, the reduce effective transconductance is the major drawback of these techniques. Though, one of the main problems that must be addressed in the LV OTA designs is to provide sufficiently large Gm. In fact, the application of LV design techniques commonly decreases the effective Gm of structure. Unfortunately, this degrades most of the desired parameters of OTA, such as speed, power, and voltage gain. Some efforts have been made to address this short come [14-20]. For instance, a positive feedback scheme is used in [14] to boost Gm, or current recycling method is utilized by [17, 19, 20] for trans-conductance and slew rate enhancement of folded cascode structures. Yet, each has its own disadvantage. For instance, structures presented in [17, 19, 20] all suffer from reduced output swing range due to the use of cascoding structures. One

accepted routine to realize dependable low voltage circuit, is to combine some low voltage techniques in an innovative manner with well-known structure. For example, using body driven transistors in well-known folded cascode structure can effectively extend common mode input range of structure. The reduce gm now can be compensated with current recycling technique which can easily integrated to the structure. Even though this adds some extra power consumption, yet it rather solves most of the problems with low voltage regime design. The only problem remains is its reduced output swing range due to the cascode output stage. This can be tolerated in supply voltages down to 1V. Nevertheless, the structure fails to operate under supply voltages less than 0.5V.

Another important parameter that degrades in LV designs is voltage gain. Beside the straight effect of reduced Gm in structure's voltage gain, this parameter is affected by other consequences, as well. Due to the reduced supply voltage, increasing the gain by cascoding is not applicable in most cases. Though, the only option remains is to use cascading [21, 22]. However, cascading increases the power consumption and design complexity. More importantly, the cascaded structures always require complex compensation networks because of the increase in the number of amplification stages and consequently high-impedance nodes [23].

A new amplifier design concept based on the second generation of current conveyor (CCII) is presented in this work. The proposed structure employs a very compact CCII structure which is especially designed to serve the proposed idea. The proposed CCII utilizes the flipped voltage follower structure to deliver some ever-interesting parameters such as low input impedance and high output impedance under very reduced power consumption. Thanks to the novel structure and compact circuit realization, the proposed structure succeeds in delivering some improved specifications. Indeed, the structure employs both cascoding and cascading to achieve very high gain values. It uses three cascading stages to boost the gain. Nevertheless, one stage of this cascading is imbedded in to the flipped voltage follower (FVF) structure that ease the compensation effort considerably. The proposed structure avoids the cascode branch in output stage to maximize the output swing range. However, the input common mode range is limited due to the use of no especial low voltage technique. Fortunately, this is not a serious challenge as it can be solved, if required, by applying some known techniques such as using bulk driven transistors.

The paper is organized into four sections. After introduction in section 1, section 2 describes the circuit realization and its performance. In section 3 the simulation results are presented. Finally, section 4 concludes the paper.

2. The proposed amplifier

2.1. FVF-based differential input stage

The differential input stage is an essential building block in any amplifier structure. This stage, conventionally, is realized by two input-transistors and a tail current (Fig. 1a). This block converts differential and even single-ended voltage signals to differential current signals, effectively. Despite some limitations such as restricted slew rate and reduced voltage headroom due to the V_{ds} requirement by the tail current, this structure, still, is very promising in amplifier structures. Here, we will look from another perspective at this block and will try to redesign it for better functionality.

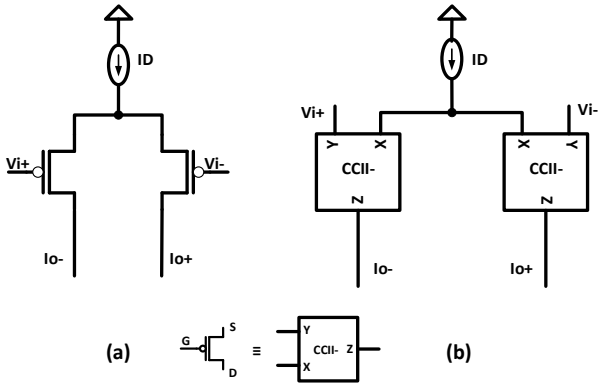

Fig.1. (a) The conventional differential input stage, (b) The current conveyor-based realization of (a)

Each transistor in Fig. 1a can be regarded as a second-generation current conveyor (CCII), where in, the terminals of gate, source, and drain correspond to Y, X, and Z terminals in CCII. Though, Fig. 1a can be redrawn as Fig. 1b.

The problem with transistors is that their characteristics are determined by technology parameters, while for the CCII, they can be set by various circuit realizations, providing extra degree of freedom for designer. For example, the trans-conductance and the voltage gain of transistor are intrinsic and given by g_m and $g_m r_o$, respectively, while for CCII, they are given by $1/r_x$ and R_o/r_x; where r_x and R_o are input and output impedance of CCII, respectively. Our goal is to advantage this perspective to configure an input stage with enhance trans-conductance and voltage gain, the degraded parameters in modern technologies. Therefore, if we can manage to have a CCII structure with $r_x<1/g_m$ and $R_o>r_o$, we can configure an input stage with trans-conductance and voltage gain higher than gm and $g_m r_o$, respectively. Nevertheless, all CCII structures are not suitable for this goal. It must be kept as simple as possible to preserve the simplicity of the traditional differential input stage. More importantly, is its frequency characteristics, which should avoid any low frequency zero and poles. Otherwise, the frequency characteristics of overall amplifier may be degraded drastically. Here we propose a CCII structure which can serve well for the purpose of writing, a flipped voltage follower (FVF) based structure.

The FVF-based CCII and the proposed FVF-based differential input stage are shown in parts (a) and (b) of Fig. 2, respectively. Enjoying from FVF structure, the proposed CCII presents a reduced input resistance r_x of $1/g_m^2 r_o$ and increased output resistance and voltage gain of $g_m r_o^2$ and $g_m^3 r_o^3$, respectively. Interestingly, the frequency characteristics of FVF structure is also very promising, where in, the non-dominant poles are located

at far beyond unity gain frequency (UGF). Besides, the power consumption is well-kept under control. It is worth noting that, although the power consumption of input stage is almost doubled, however, as this stage consumes a small fraction of overall amplifiers' power, the power consumption of the whole amplifier does not affect much.

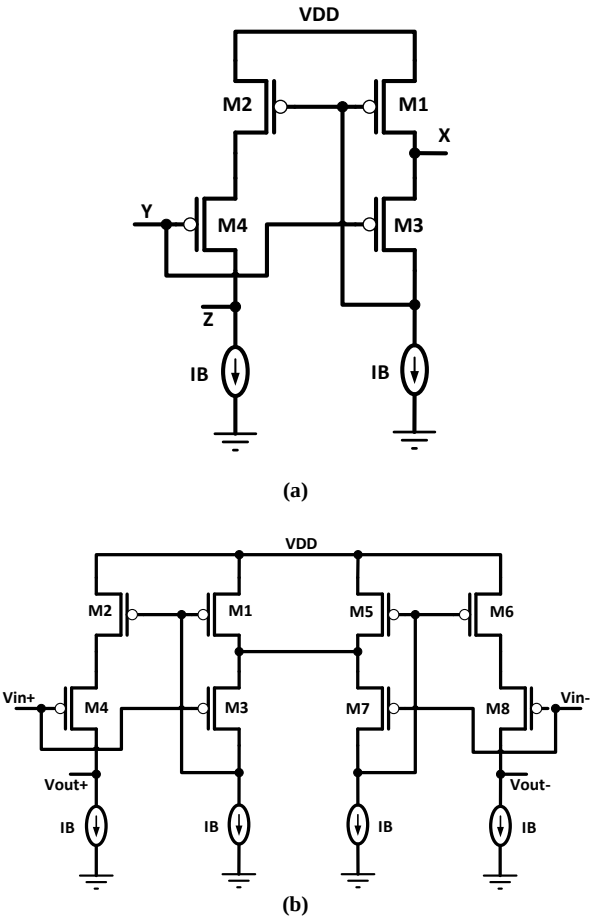

Fig. 2. (a) FVF-based CCII, (b) differential input stage based on FVF-based CCII

To further discuss the performance of FVF-based differential input stage, let us assume that a differential signal is applied to its inputs. This differential signal deviates the structure from balanced condition and causes a current flowing from M1 to M5. This current is mirrored by M2 and M6 correspondingly and delivered to the outputs through M4 and M8. As the X node impedance of FVF structure is very low ($1/g_m^2r_o$), the signal due to the differential input voltage will be considerably high (about $g_m^2r_o$). Now consider we apply a common mode signal to structure's inputs. At this condition, due to the large degeneration output resistors of M1 and M5, the current signal that is generated and then transferred to the structure's outputs will be extremely low (ideally zero). This promises a very high value of CMRR for the proposed FVF-based differential input stage.

The transistor-level realization of the proposed FVF-based gm-enhanced amplifier is presented in the following section.

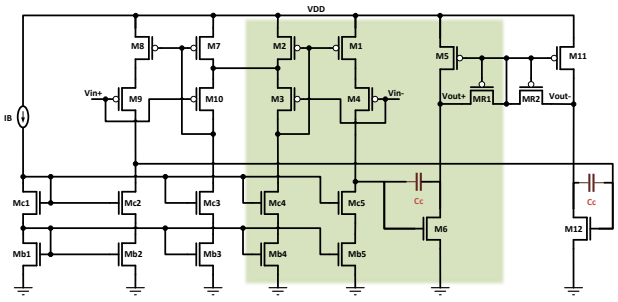

Fig. 3. Transistor level implementation of the proposed amplifier

2.2. Proposed FVF-based gm-enhanced amplifier

The transistor-level realization of the proposed FVF-based gm-enhanced amplifier is depicted in Fig. 3. One half-circuit of the overall fully differential structure is shaded in the picture (of Fig. 3), which is composed of compensation capacitor of Cc and transistors M1-M6, Mc4-Mc5, Mb4-Mb5, and MR1. Considering one half-circuit of the structure (the shaded one), transistors M1-M4 in coordination with biasing transistors of Mc4-Mc5 and Mb4-Mb5 configure the first stage of amplifier. Whereas the transistors M5-M6 configure the second stage. The transistor MR1 with the help of MR2 (its counterpart in other half-circuit) configures local common-mode feedback to separate the common mode signal from differential mode one and also to set the common mode voltage at proper voltage value. The two half-circuits of structure act in a collaborative manner to configure fully differential well-balanced amplifier structure. Performing some calculations, the common-mode and differential-mode voltage gains are given by the following relations for the whole amplifier. By calculating the output voltages for differential mode and common mode voltages from (1) and (2) respectively, we can obtain the differential mode and common mode voltage gains given by (3) and (4), respectively. In fully differential amplifiers, the common mode voltage gain is obtained by calculating the voltage gain for either positive or negative output voltage; here, we used the positive voltage for this sake.

These relations show that the differential mode voltage gain is given by $(g_mr_o)^4$, approximately; while the common mode gain can be reached to zero, providing that a perfect matching between M1 and M2 can be made. Even if we consider a 10% mismatch between these two transistors, the common mode voltage gain is given by $(g_mr_o)/10$, approximately. This is at least 4 orders of magnitude less than differential mode voltage gain, approximately. These calculations promise very high attainable CMRR values.

$$\frac{V_{out+}}{V_{id}} \approx \frac{1}{2} g_{m1}g_{m3}g_{m6}r_{o3}\left(g_{m4}r_{o1}r_{o4} \parallel g_{mc5}r_{ob5}r_{oc5}\right)\left(r_{o5} \parallel r_{o6}\right)$$
$$\frac{V_{out-}}{V_{id}} \approx -\frac{1}{2} g_{m8}g_{m10}g_{m12}r_{o10}\left(g_{m9}r_{o8}r_{o9} \parallel g_{mc2}r_{ob2}r_{oc2}\right)\left(r_{o12} \parallel r_{o11}\right) \quad (1)$$

$$\frac{V_{out+}}{V_{ic}} \approx \frac{g_{m6}}{g_{m5}}\left(\frac{1}{r_{o1}}-\frac{g_{m1}}{g_{m2}r_{o2}}\right)\left(g_{m4}r_{o1}r_{o4} \parallel g_{mc5}r_{ob5}r_{oc5}\right)$$
$$\frac{V_{out-}}{V_{ic}} \approx \frac{g_{m12}}{g_{m11}}\left(\frac{1}{r_{o8}}-\frac{g_{m8}}{g_{m7}r_{o7}}\right)\left(g_{m9}r_{o8}r_{o9} \parallel g_{mc2}r_{ob2}r_{oc2}\right) \quad (2)$$

$$A_{vd}=\frac{V_{out+}-V_{out-}}{V_{id}} \approx \frac{1}{2}g_{m1}g_{m3}g_{m6}r_{o3}\left(g_{m4}r_{o1}r_{o4} \parallel g_{mc5}r_{ob5}r_{oc5}\right)\left(r_{o5} \parallel r_{o6}\right)$$
$$+\frac{1}{2}g_{m8}g_{m10}g_{m12}r_{o10}\left(g_{m9}r_{o8}r_{o9} \parallel g_{mc2}r_{ob2}r_{oc2}\right)\left(r_{o12} \parallel r_{o11}\right) \quad (3)$$

$$A_{vc}=\frac{V_{out-}}{V_{ic}}=\frac{V_{out+}}{V_{ic}} \approx \frac{g_{m6}}{g_{m5}}\left(\frac{1}{r_{o1}}-\frac{g_{m1}}{g_{m2}r_{o2}}\right)\left(g_{m4}r_{o1}r_{o4} \parallel g_{mc5}r_{ob5}r_{oc5}\right) \quad (4)$$

$$\overline{V_{n,in}^{\,2}} \approx \frac{\overline{I_{1,n}^{\,2}}+\overline{I_{B4,n}^{\,2}}+\overline{I_{B5,n}^{\,2}}}{g_{m1}^{\,2}g_{m3}^{\,2}g_{mc4}^{\,2}r_{dsc4}^{\,2}r_{dsb4}^{\,2}}+\frac{\overline{I_{4,n}^{\,2}}}{g_{m1}^{\,2}g_{m3}^{\,2}g_{m4}^{\,2}g_{mc4}^{\,2}r_{ds1}^{\,2}r_{dsc4}^{\,2}r_{dsb4}^{\,2}}+\frac{\overline{I_{3,n}^{\,2}}}{2g_{m3}^{\,2}} \quad (5)$$

2.3. *Noise Analysis*

It is well-established that the noise performance of the two-stage circuit is dominated by the first stage. To this end, the noise contributors in the half-circuit of the first stage are depicted in Fig. 4. Using the schematic of Fig. 4, the input referred noise voltage is given as (5).

The relation (5) shows that the noise performance of structure is mainly dominated by input-transistor M3 (M10). The noise contribution of transistor M2 (M7) is eliminated from the outputs due to its common mode appearance, thus generates no differential signal in the output.

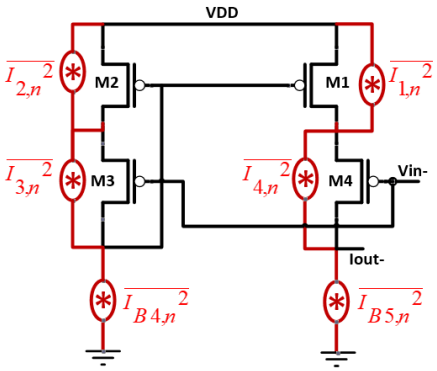

Fig. 4. The half-circuit noise model for the input stage of proposed structure

2.4. *The common-mode feedback, compensation network*

In general, any fully differential structure needs a common-mode feedback circuit to stabilize the output common mode voltage of the overall structure. The reason behind is that unlike for the single-ended amplifiers, for differential output amplifiers the general feedback fails to stabilize the output common-mode voltages. In the proposed structure, the CMFB circuit is accomplished by the MR1 and MR2 which act as large resistors and average and feed the common-mode signal back to the circuit. The CMFB circuit employed in the proposed structure is absolutely power and area efficient. It introduces no extra power to the circuit. Besides, the large resistors are implemented with two small transistors that occupy negligible area. In addition to CMFB in the output stage, the circuit effectively suppresses the common mode input signals, as well. As is discussed in previous section, the common mode signals experience very low amplification gain compared to the differential mode ones.

Referring to the schematic of the proposed circuit in Fig. 3, the dominant poles of amplifier can be estimated intuitively. In brief, the two most dominant poles of the structure are estimated to be located at gate and drain of M6 (M12). The first pole which is located at the gate of M6 (M12), is mainly due to the very large output impedance seen from this node and relatively large capacitance of M6 (M12). This pole value is about $P_1 \approx -1/(r_{o1}r_{o4}g_{m4}||r_{ob5}r_{oc5}g_{mc5})(C_{gs6}+C_{gd6}(1+g_{m6}(r_{o6}||r_{o5})))$. The second pole is mainly due to the large load capacitance and relatively large output impedance. This pole value is about $P_2 \approx -1/(r_{o6}||r_{o5})C_L$. The proposed circuit simply adopts the miller compensation network to compensate the circuit for desired phase margin at required amplification gain (C_C=1pF). Applying Miller compensation relocates the poles in $P_1' \approx -1/(r_{o1}r_{o4}g_{m4}||r_{ob5}r_{oc5}g_{mc5})(C_{gs6}+(Cc+C_{gd6})(1+g_{m6}(r_{o6}||r_{o5})))$ and $P_2' \approx -g_{m6}/C_L$, respectively. It is worth noting that as the proposed circuit is devoted for application as preamplifier stage in signal acquisition systems, it will not be compensated for unity-gain feedback condition. This enables the structure to achieve very high operating bandwidth under reduced power consumption along with precise amplification gain; thanks to its very high open loop gain. Yet, it is worth noting that the compensating for unity-gain feedback condition would require large capacitors in compensation network. Which fortunately is not applicable to the current design due to its target application.

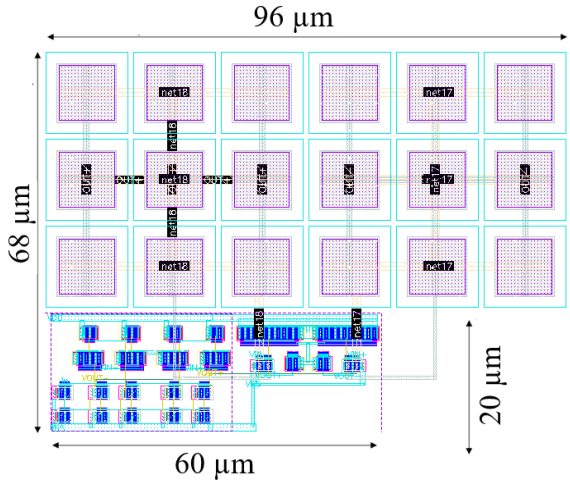

Fig. 5. The layout view of the proposed current push-pull based OTA

3. Simulation Results

The post-layout simulations are carried out using TSMC 180nm, MS/RF, 1P6M, CMOS technology utilizing 0.6V power supply. The transistor aspect ratios and bias current are provided in Table I. The layout view of the proposed structure is given in Fig. 5. The structure occupies about 0.006 mm^2 with a core area of 0.001 mm^2. Due to the low supply voltage and very low biasing currents, all transistors are forced to operate in subthreshold region. The frequency performance is plotted in Fig. 6. This figure shows the magnitude and phase of the amplifier over the frequency range. From this figure, the DC gain of the proposed OTA is evaluated to be 141.5dB. As is stated earlier, the circuit is proposed to be used as a pre-amplifier in applications with high and precise voltage gains. Therefore, the phase margin should be checked for 60 dB which is the gain of feedback loop. Hence, here the amplifier is compensated for 60 dB feedback gain. This prevents bandwidth reduction due to unnecessary compensation for unity gain configuration. The feedback network can simply be realized by capacitors or resistors (here 10 pF and 10 fF capacitors).

Table I. The bias currents and transistor aspect ratios

Transistor	W/L (µm/µm)
Mc1, Mb1	2/0.54
Mc2-Mc5, Mb2-Mb5, M1, M2, M7, M8, MR1, MR2	4/0.54
M3, M4, M9, M10	8/0.54
M6, M12	3.4/1
M5, M11	20/0.54
Bias Current	**Value (nA)**
IB	2.5

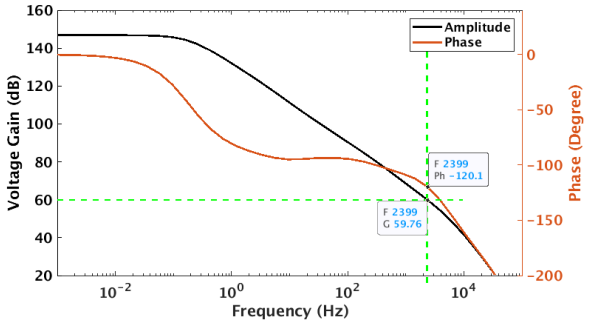

Fig. 6. The open-loop voltage gain frequency response of the proposed structure

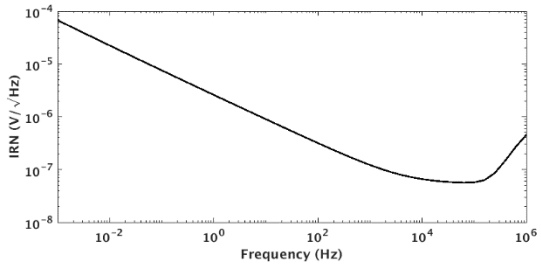

Fig. 7. The input-referred noise characteristic of proposed OTA

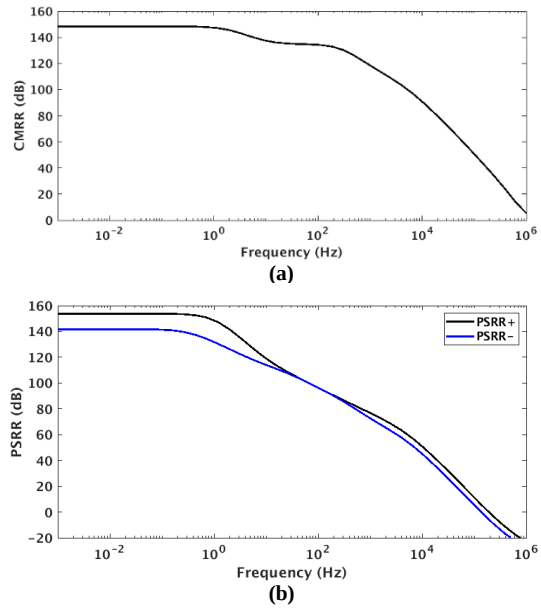

Fig. 8. The common-mode (a) and power supply (b) rejection characteristics of the proposed OTA

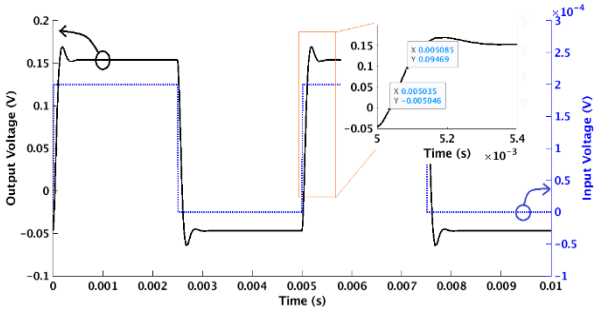

Fig. 9. The transient large-signal step response of proposed OTA in 60 dB gain configuration

The input referred noise characteristic of circuit is depicted in Fig. 7. This figure shows that the proposed structure delivers an acceptable noise performance in its

operating frequency range. The value of IRN is evaluated to be 0.12μV/√Hz at frequency of 1kHz. The CMRR and PSRR performance of the proposed structure are pictured in parts (a) and (b) of Fig. 8, respectively. This figure shows that both parameters are well satisfactory. The very large value of the CMRR makes the proposed structure very suitable for circuits with biomedical applications. This mainly comes from the common-mode feedback and degeneration circuits.

The transient step-response of the proposed circuit configured in 60dB feedback gain is depicted in Fig. 9. The step size of input voltage was 0.2mV. This figure shows that the proposed structure delivers a fast rise and settling time in a stable fashion. From this figure the circuit parameters such as slew rate and settling time are extracted to be 1.9mV/μs and 430μs, respectively. This relatively high value of slew rate is mainly due to the class AB operation of structure.

To evaluate the performance of the proposed structure against process uncertainties, the Monte Carlo simulations are conducted with 1000 runs and the results are pictured in histograms of Fig. 10 and Fig. 11. The DC voltage gain is shown in Fig. 10 (a) and the CMRR is pictured in Fig. 10 (b). The circuit simulation for open loop bandwidth is pictured in Fig. 11 (a) while the simulation for closed loop bandwidth is depicted in Fig. 11 (b). The results are very promising, showing no considerable deviation (small standard deviation, σ) from the mean value, μ.

Further investigation of circuit performance against process variations is performed by corner simulations. Therefore, the post-layout simulations are conducted in all five corners and at various operating temperatures. The simulated corners were TT, FF, SS, FS, and SF; wherein, T, F, and S stand for typical, fast and slow corners, respectively for NMOS and PMOS transistors. The results are summarized in Table II. This table includes the Monte Carlo (MC) simulation results, as well. From Table II, it can be noticed that even at the worst condition, the DC gain and CMRR parameters remain higher than 131.3dB and 135.9dB, respectively. This promises that the key parameters of the structure are well-robust against temperature and process variations. The performance parameter comparison of the proposed structure with some relevant recent works is given in Table III. From Table III, it can be noticed that the proposed OTA delivers better performance compared to most of the works in terms of some interesting merits such as DC gain, gain bandwidth, and CMRR. Therefore, the proposed OTA is best suited for low noise, low power and relatively fast applications. The following figures of merit are defined to compare the performance of the proposed structure with other work [5, 6, 24, 25].

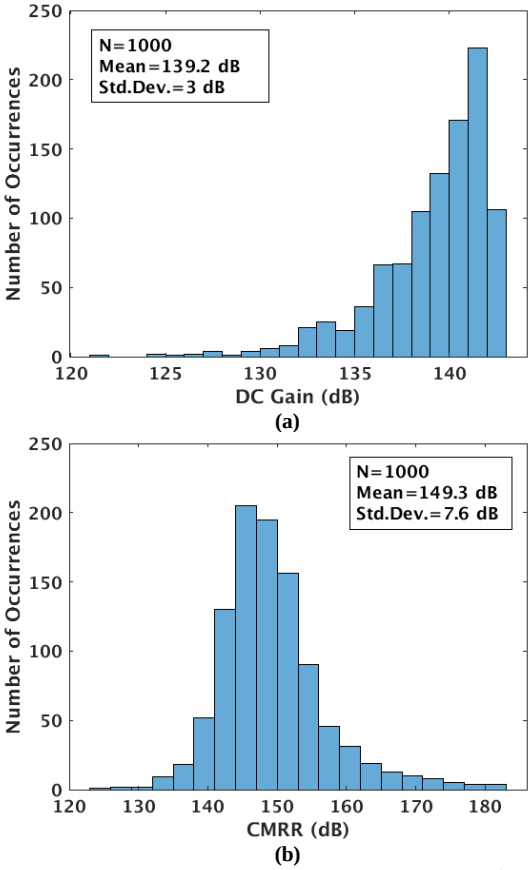

Fig. 10. The post-layout Monte Carlo simulation results for (a) DC voltage gain, (b) CMRR

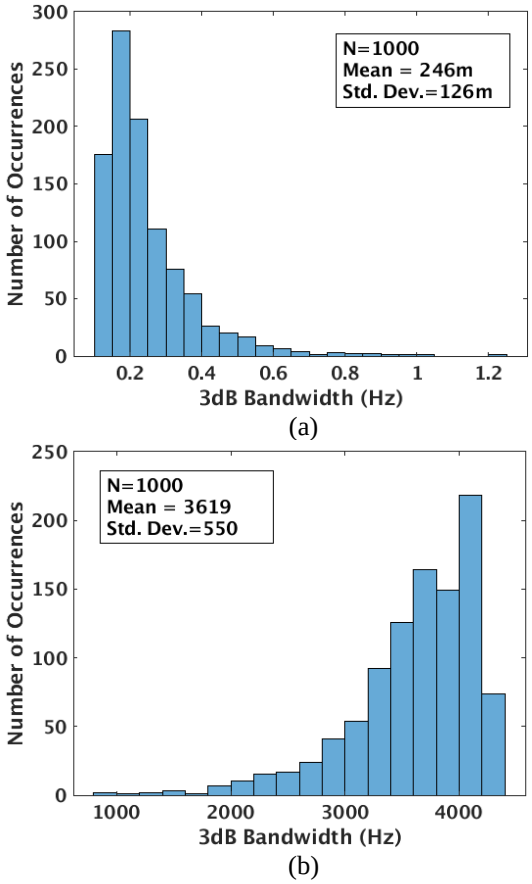

Fig. 11. The post-layout Monte Carlo simulation results for (a) Open loop bandwidth, (b) Closed loop bandwidth at 60 dB feedback gain

$$FOM_S = 100 \times \frac{G.BW.C_L}{I_{DD}} \times \frac{V_{THN} + V_{THP}}{V_{DD}} \quad (6)$$

$$FOM_L = 100 \times \frac{SR.C_L}{I_{DD}} \times \frac{V_{THN} + V_{THP}}{V_{DD}} \quad (7)$$

$$FOM_{SP} = FOM_S \times \frac{A_{v0}}{1000} \quad (8)$$

$$FOM_{LP} = FOM_L \times \frac{A_{v0}}{1000} \quad (9)$$

Comparing the performance of various works is rather hard and complex. The reason is that the circuit design procedure is a trade-off problem. Therefore, each work shows a superior performance in some parameters but fails to combat in term of other parameters. This suggests the definition and usage of some FOMs that helps to compare the overall performance of two or even more structures, appropriately. Using the presented FOMs and based on the calculated values form Table 3, the proposed OTA outperforms the other works in three out of four defined figures of merit, including FOM_S, FOM_{SP}, FOM_{LP}.

Table II. The Post-layout simulation results of the OTA performance over temperature and process variations

Corner	TT @ 27°C	FF @ 0°C	SS @ 85°C	FS @ 27°C	SF @ 27°C	MC	
						μ*	σ*
DC gain (dB)	141.5	135.8	134.7	131.3	134.6	139.2	3
CMRR (dB)	148.3	149.6	164.7	135.9	175.5	149.3	7.6
PSRR+ (dB)	153.7	158.4	148.8	137.2	150.3	-	-
PSRR- (dB)	141.3	137	137.3	129.1	137.3	-	-

* μ: Mean value
* σ: Standard deviation

Table III. The summery of OTA parameters compared with some recent relevant works

Parameter	This Work	[26]	[3]	[5]	[6]	[27]	[28]	[29]	[25]*	[24]*	[13]*	[30]*
V_{DD} (V)	0.6	0.5	0.3	0.4	0.4	0.5	0.5	0.6	0.25	0.3	0.3	0.9
P_{diss} (μW)	0.15	0.026	0.051	2.6	0.3	28	0.3	0.4	0.018	0.017	0.013	24.3
C_L (pF)	5	15	5	5	5	20	5	15	15	20	30	10
DC gain (dB)	141.5	67.8	60	72.6	81.37	65	60	82	60	65.8	64.7	65
Open loop BW (Hz)	1.83	1.33	70	76.6	23.9	309	27	1.5	1.88	1.4	1.68	562
PM (°)	60**	68.9	53	56	59.2	50	69	60	52.5	61	52	60
SR (mV/μs)	1.9	0.84	25	212	125	230	-	12	0.77	7.1	1.9	250
IRN (nV/√Hz) at 1kHz	121.8	560	2820	173	213	432	2000 @ 0.1kHz	160	#3300	-	-	65
CMRR (dB)	148.3	-	126	110.7	126	86	53.15	130	-	72	110	45
PSRR (dB)	153.7	-	91	103	79.1	76	-	-	-	62	56	55
1% Ts (μs)	430	635	49.4	6.4	11	-	-	-	-	104	446	1.8
Area (mm^2)	0.006	-	0.003	0.013	0.005	0.052	-	-	0.083	0.008	0.008	0.014
FOM_S (V^{-1})	72666	188	411	63	467	39.3	45	60	67.4	349	669	561
FOM_L (V^{-1})	6.3	48.4	245	41	208	16.4	-	45	36.8	856	438	140
FOM_{SP} (V^{-1})	>863*10^6	451	411	271	5468	66.8	45	750	67.4	680	1149	997
FOM_{LP} (V^{-1})	>73000	116.1	411	168.6	2435	113.6	-	562.5	36.8	1669	752	249
Technology (nm)	180	180	65	180	180	180	180	180	130	180	180	350

* Measurement results
# Thermal Noise
** for 60dB voltage gain

4. Conclusion

A High-gain, fully-balanced preamplifier was presented in this paper. The proposed structure advantages flipped voltage follower scheme to achieve a compact current conveyor with very low input impedance. The presented current conveyor was used as a core element to realize a high-gain, gm-enhanced trans-conductance amplifier. The Spectre Post-layout simulations with TSMC 180nm CMOS technology file have been performed to validate the performance of the proposed amplifier. The proposed amplifier exhibits an open loop DC gain of 141.5dB and 3-dB frequency bandwidth of 2.4kHz at 60dB closed-loop configuration. The load capacitance is set to be 5pF. The proposed structure also delivers high CMRR and PSRR values of 148.3dB and 153.7dB, respectively. To investigate the performance of the design over process and temperature variations, the Monte Carlo and corner simulations are performed.

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