Reference spur suppression in the Integer-N frequency synthesizers by reducing periodic ripples amplitude on the VCO control voltage

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Abstract
To achieve a low reference spur for an Integer-N frequency synthesizer, a new spur reducing technique was proposed. To reduce the size of periodic ripples on the VCO control voltage, the low pass filter, and the charge pump were added with a spur reduction system. By lowering the amplitude of the periodic ripple on the VCO control voltage, we managed to lower the reference spur. The introduced technique removes the necessity to decrease bandwidth and CVO gain reference spur suppressing. To demonstrate the effectiveness of the proposed structure, a 2.06 – 2.22 GHz frequency synthesizer was used and the 180-nm CMOS technology was used for post-layout simulation. The proposed frequency synthesizer represents the reference spur of -85.84 dBc at 20 MHz offset and phase noise of -108dBc/Hz at 200 kHz offset frequency also it is locked after 2.8us while occupied 0.35 mm2 of the chip area.

Keywords
Spur suppression, reference spur, voltage controlled oscillator (VCO), and integer-N frequency synthesizer

1. Introduction

Reference spurs degrade the efficiency of the Integer-N frequency synthesizer considerably. This is caused by the periodic ripples on the control voltage of the voltage-controlled oscillator (VCO). The non-idealities of the phase-frequency detector (PFD) and the charge pump (CP) circuits like the difference between the up and down currents, feedthrough, leakage of the CP current, and timing difference of the PFD outputs signals are the main sources of periodic ripples. The amount of performance degradation is measured by subtracting the strength of the spur at the offset frequency f_{ref} from the carrier. The reference spur magnitude to the carrier magnitude ratio is given as [1]:

$$\frac{A_{spur}}{A_{carrier}} = \frac{1}{2}\frac{K_{VCO} \times V_m}{2\pi f_{ref}} \quad (1)$$

where V_m is the size of the ripple, K_{VCO} and f_{ref} refer to the VCO gain and the reference frequency.

Equation (1) implies that the size of the spur has a linear relationship with the magnitude of the ripple and the VCO gain, while it is proportioned to the reference frequency inversely. Several techniques are available to decrease the effects of the reference spur on frequency synthesizers. One of the techniques is to lower the VCO gain [2-5] that restricts the range of tuning frequency. To compensate for the frequency tuning range, other techniques like the switched capacitor [1], [6-7], or dual path-controlled VCO [8-9] are required.

Utilizing higher-order loop filters decreases ripple on the VCO control voltage [10-11], however, the complexity and instability are increased by higher order-loop filters. In addition, a narrow loop bandwidth can decrease the reference spur level [12], but the loop bandwidth reduction increases the settling time, the effect of the VCO phase noise at the output spectrum, and the on-chip filter area.

To increase reference spur frequency, a change distribution mechanism was used on VCO control voltage in [13]. Thus, the size of the reference spur is lowered efficiency using the loop filter transfer function. Through this, spur frequency shifting is achieved using several delayed phase-frequency detector-charge pump (PFD-CP) paths that increase the mismatch sensitivity between multiple paths. To achieve spur frequency shifting, cascade phase-locked loops (PLL) and a technique for sampling the input reference sine wave with a CVO square wave were used in [14]. The two techniques achieve a notable decrease in the sum of phase

noise given the excessive noise added by additional elements.

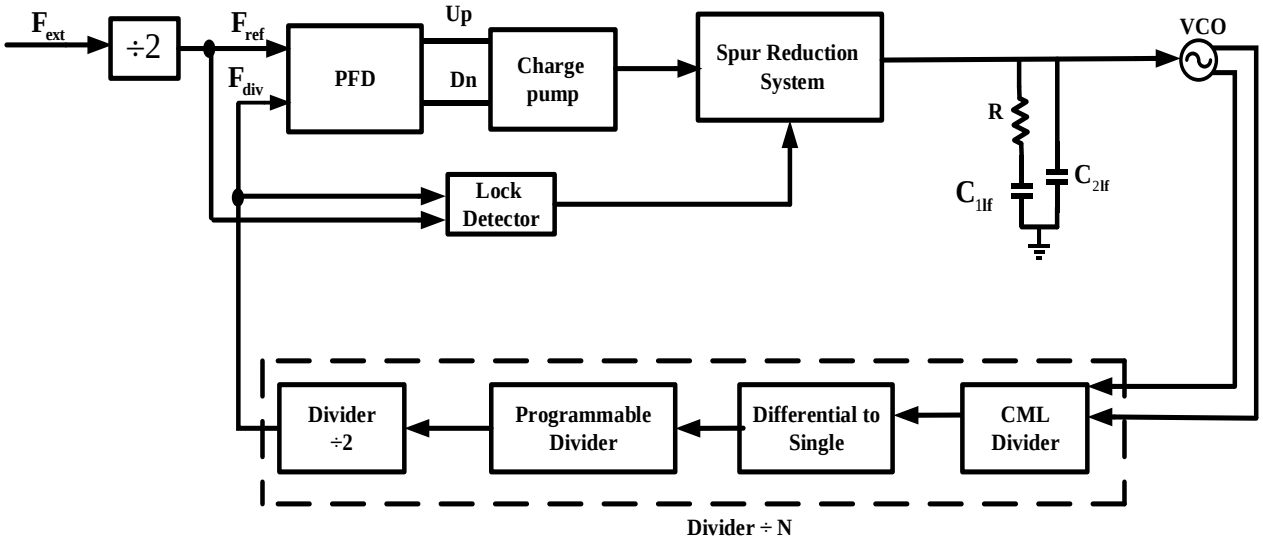

Fig. 1. The introduced frequency synthesizer

The methods to randomize the charge distribution in [16-19] decrease the reference spurs. Another technique to lower the reference spur is to shift the offset frequency higher than the reference frequency [20-21]. In [20], a two-path switched capacitor network is inserted between the CP and the low-pass filter (LPF) to double the spur frequency. In [21-22], the PFD and the CP are added with a booster block of spur frequency to shift the spur frequency to multiple the reference frequency. For the sampling purpose, self-feedback injection-locked ring oscillator, and pseudo-random injection-locked technique were used in [23]; still, this approach requires a great deal of energy as two VCOs are used in the technique. To lower the reference spurs, authors in [24] used a sampler between the LPF and the VCO. The control voltage is sampled through each reference period, which leads to a decline in reference spur. The instability of the loop is the main disadvantage of this method, which is due to the sampler delay.

A novel approach was proposed based on lowering the size of periodic ripples of the VCO control voltage to decrease the tradeoff of low spur level and the wide bandwidth of LPF so that the reference spur is lowered notably.

The rest of the article is as follows: The proposed circuit is discussed and the major elements are given in Section 2. Section 3 gives the post-layout results of the simulation, and the conclusion is given in section 4.

2. Circuit Description

The introduced low-spur Integer-N frequency synthesizer is illustrated in Fig.1. The architecture contains a standard frequency synthesizer, a spur lowering system, and a lock detector. The key idea is to attenuate the size of the periodic ripples on the VCO control voltage.

Considering a second-order filter, the following is the loof filter transfer function:

$$F(s)=\frac{1+sC_{1lf}R}{s^2C_{1lf}C_{2lf}R+s(C_{1lf}+C_{2lf})}=\frac{1+\frac{s}{w_z}}{s(C_{1lf}+C_{2lf})(1+\frac{s}{w_p})} \quad (2)$$

where $w_z=\frac{1}{RC_{1lf}}$ and $w_p=\frac{1}{R\left(C_{1lf}\parallel C_{2lf}\right)}$ represent the zero of the loop filter and the pole respectively.
The VCO output is expressed as [27]:
Therefore, the size of the reference spurs derived as:

$$\begin{aligned}V_{out}&=A_{VCO}\cos\left(w_0t+K_{VCO}\int_0^t V_m\cos\left(w_{ref}t\right)dt\right)\\&=A_{VCO}\cos\left(w_0t+\frac{K_{VCO}V_m}{w_{ref}}\sin\left(w_{ref}t\right)\right)\\&\approx A_{VCO}\cos\left(w_0t\right)+A_{VCO}\frac{K_{VCO}V_m}{2w_{ref}}\cos\left(w_0-w_{ref}\right)t\\&+A_{VCO}\frac{K_{VCO}V_m}{2w_{ref}}\cos\left(w_0+w_{ref}\right)t\end{aligned} \quad (3)$$

Therefore, the size of reference spurs is:

$$A_{spur}=A_{VCO}\frac{K_{VCO}V_m}{2w_{ref}} \quad (4)$$

Therefore, according to the above equation, the size of the reference spur is relative to the size of the ripple on the VCO control voltage. As a result, in the new structure, the idea of reducing the size of ripples on the VCO control voltage is used to lower spurs.

In the proposed structure, a lock detector is used to indicate lock status. When the circuit is not locked, the spur reduction system is disabled and the proposed structure works similarly to standard frequency synthesizers. If the feedback signal and the reference input have any phase inconsistency detected by aA PFD, then an error signal is generated. Based on the error signal, the CP can increase/decrease the amplitude of the change pumped to LPF. The CVO control voltage is tuned using this charge. In the case of standard frequency synthesizers, parameters of loop design control the size of the ripple on the VCO control voltage. The size of the ripples on the control voltage is decreased and, therefore, reference spurs are significantly suppressed.

2.1. Spur Reduction System

A spur reduction system is added between the CP and LPF to reduce the amplitude of the periodic ripples which includes three equal capacitors C_1, C_2, C_3 and several switches controlled by pulses S_1, S_2, S_3 and S_4 which are implemented by the input reference signal, the external signal, and many logic circuits as illustrated in Fig. 2.

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The 20 MHz input pulse is obtained by dividing by 2 the external pulse of 40 MHz and the timing diagram of the switches is presented in Fig. 3.

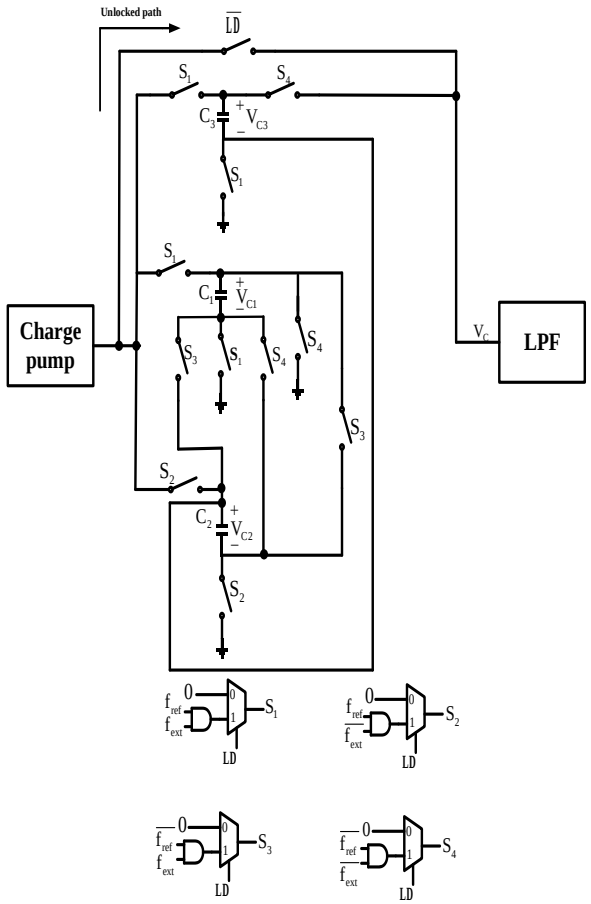

Fig. 2. Spur reduction system

When S_1 turns on, the charge is simultaneously transferred from the CP to the equal capacitors, C_1 and C_3 while the other switches are off. Therefore, capacitors C_1 and C_3 are separated from the LPF, and no charge is transferred to it. At this time, the voltage of capacitors C_1 and C_3 is equal to:

$$V_{C1} = V_{C3} = V_{lock} + V_m \tag{5}$$

Then, S_1 turns off and S_2 turns on, as represented in Fig.3, the charge without ripples is transferred from the CP to the capacitor C_2. Therefore, the voltage of the capacitor C_2 is equal to:

$$V_{C2} = V_{lock} \tag{6}$$

When the switch S_3 is on, the two capacitors C_1 and C_2 connect in parallel inversely, so the resulting voltage is half the voltage difference between capacitors C_1 and C_2. In this case, the voltage of capacitors C_1 and C_2 is equal to:

$$V_{C1} = -V_{C2} = \frac{q}{2C} = \frac{C_2V_2 - C_1V_1}{2C} = \frac{V_m}{2} \tag{7}$$

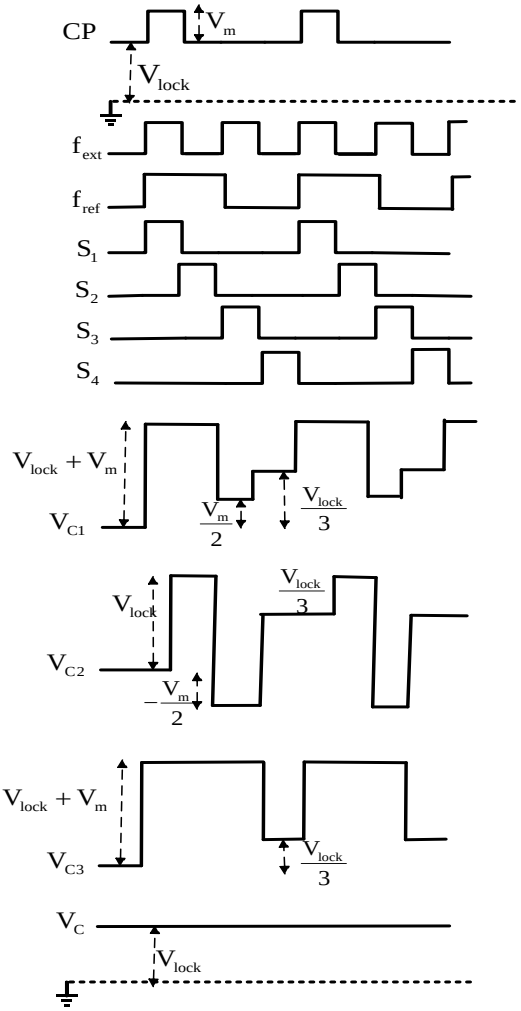

Fig. 3. The timing diagram of the switches

Then, S_3 turns off and S_4 turns on. In this case, two capacitors C_1 and C_2 are series so the voltage difference created in the previous step is doubled and added to the voltage created in the capacitor C_3 in phase S_1 concurrently. As a result, the ripple is removed at the VCO control voltage and the reference spur is reduced.

$$V_C = V_{C3} + V_{C1} + V_{C2} = V_{lock} + V_m - \frac{V_m}{2} - \frac{V_m}{2} = V_{lock} \quad (8)$$

Since the switches are implemented by complementary metal-oxid semiconductor (CMOS) transistors they are designed in layout to reduce the injection of charge, clock feedthrough, and mismatch effects in switches and capacitors.

2.2. Lock detector

The lock detector is a key circuit in the proposed frequency synthesizer since it determines when the spur reduction system should be active. The block diagram of the lock detector is illustrated in Fig. 4. It has two D-flip-flops and an OR gate. When the difference of phase in the reference signal f_{ref} and the divider output signal f_{div} is within $\pm t_d$, the lock detector will generate a high pulse to enable the spur reduction system. Otherwise, the output of the LD is low.

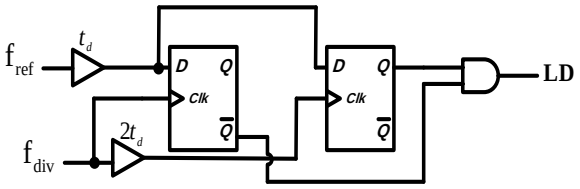

Fig. 4. The lock detector block diagram

2.3. Programmable Divider Circuit

The constituent elements of a programmable frequency divider are differential to current mode logic (CML) divider that is divided by 2, the single-ended circuit, a divide by 2 true single-phase clock (TSPC) divider and a multi-modulus divider. Figure 5 illustrates the divide by 2 CML circuits. The signals should be converted into single-ended ones for the following processes because the output of the CML circuit is differential. Thus, differential to single-ended was used.

Figure 6 illustrates the structure of a programmable multi-modulus frequency divider. It has four cascaded stages of a 2/3 divider cell. The following gives the ratio of output divider with modulus bits:

$$\text{Divider ratio} = 2^4 + 2^3 p_3 + 2^2 p_2 + 2^1 p_1 + 2^0 p_0 \quad (9)$$

The equation shows that the division ratios are in the 16-31 range. The bits program of modulus is $p_3p_2p_1p_0$=1011 to divide by 27.

2.4. Remaining Circuits

There are different ways to implement a VCO. The two common types of VCOs include ring VCOs and LC VCOs. Compared to ring VCOs, LC VCOs demonstrate better phase noise performance [25-26]. This is why the proposed structure uses the LC VCO. A schematic view of the VCO is shown in Fig.7. The VCO tenable range is between 2.08 to 2.22 GHz with a gain of 200MHz/V.

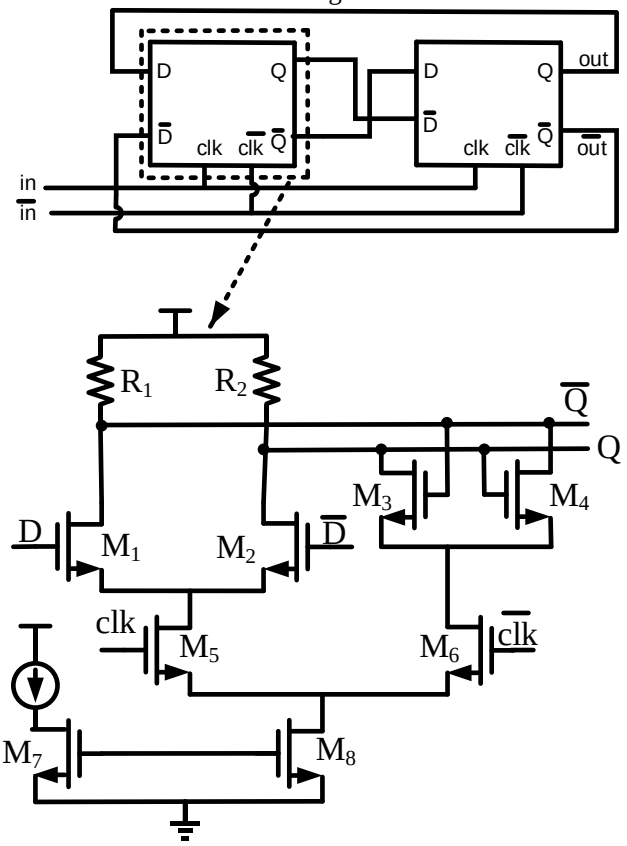

Fig. 5. CML Divide-by-2 structure

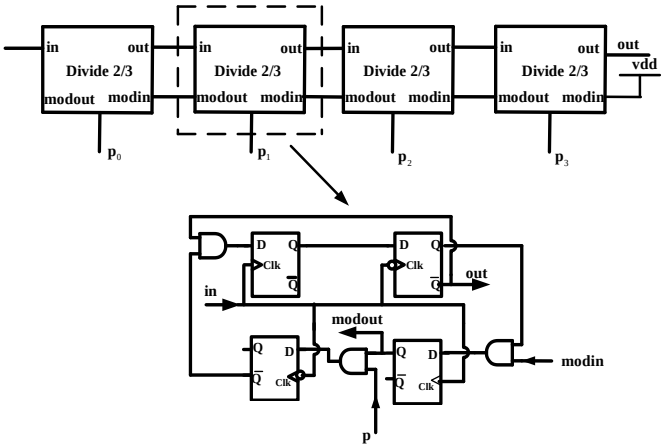

Fig. 6. Multi-modulus frequency divider structure

The phase and frequency between the divider output clock and the reference input clock are compared by PFD. It yields two up and down pulses using the difference of phase of two input signals. Fig. 8 displays the implementation of PFD consisting of NAND, standard logic gates, and an inverter.

3. Results

Using 180nm CMOS technology and 1.8V supply voltage, the layout and post-layout simulation results of

the proposed circuit are given as a way to check the presented idea. The input reference signal is 20 MHz, which is obtained by an external 40 MHz pulse, and, the VCO gain is 200 MHz/v ensued by the divider of which the division ratio N of 108.

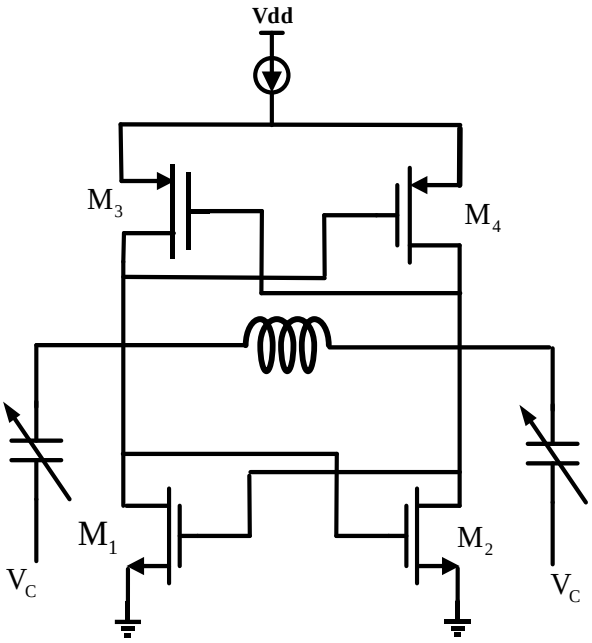

Fig.7. Circuit schematic of LC VCO

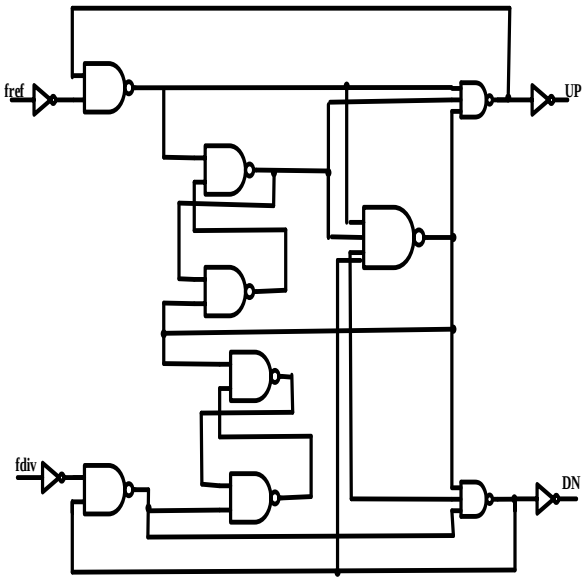

Fig. 8. PFD implementation

To achieve the level of reference spur, we recorded the synthesizer output frequency in the locked state the signal power spectral density (PSD) is determined using an FFT with 2^{19} points following convolving with the hamming window [27]. The layout of the introduced frequency synthesizer is illustrated in Fig. 9, which occupies $0.462 \times 0.749 mm^2$ of chip area.

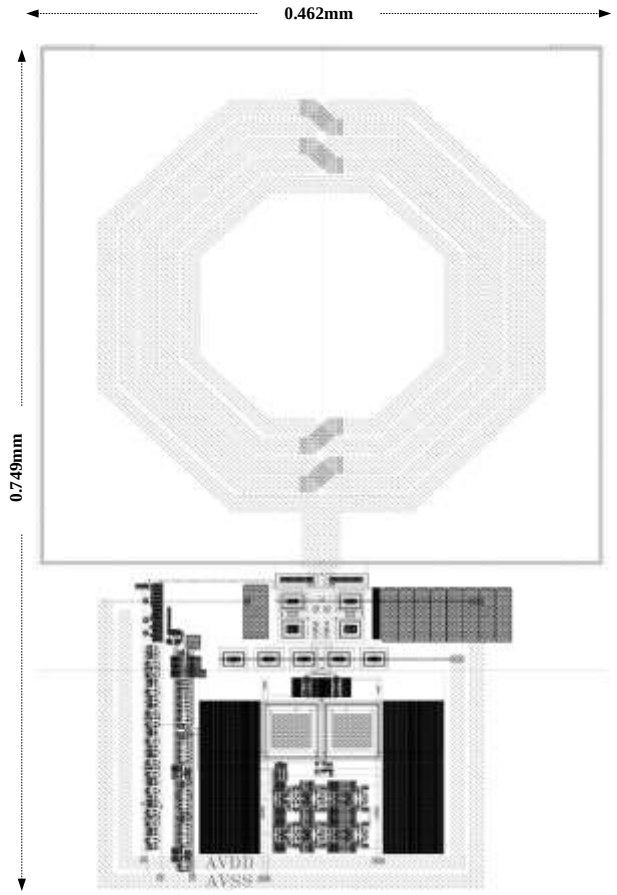

Fig. 9. The proposed frequency synthesizer layout

Figures 10&11 illustrate the results of the simulation of the VCO control voltage of the conventional frequency synthesizer and the introduced frequency synthesizer respectively. The peak-to-peak amplitude of the VCO control voltage ripple in the proposed frequency synthesizer is 9.034mV, which is about 32mV less than that of the conventional frequency synthesizer. The output of the introduced synthesizer lock detector is illustrated in Fig. 12. The synthesizer settling time is about 2.8us .

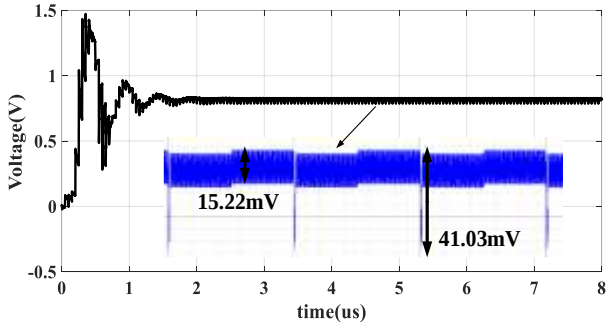

Fig. 10. The VCO control voltage of the conventional frequency synthesizer

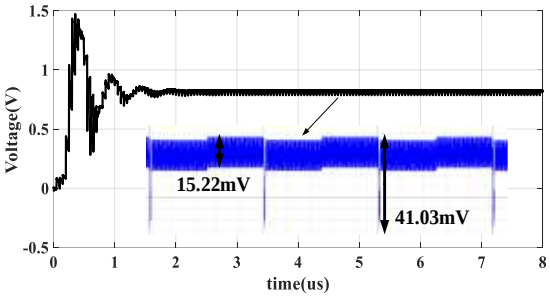

Fig. 11. The VCO control voltage of the proposed frequency synthesizer

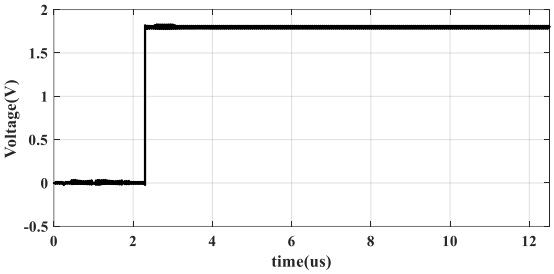

Fig. 12. Lock detector

The standard frequency synthesizer output spectrum is illustrated in Figure 13. To measure the reference spur, the difference of the carrier and the spur at a 20 MHz frequency offset is used, which is -38.9 dBc. The introduced frequency synthesizer spur level is equal to 85.84 dBc (Fig. 14). Thus, the introduced structure can increase the spur level to 46.94 dB above the standard frequency synthesizer. The proposed frequency synthesizer has been simulated with process corner variations. The process corners that have been considered are Fast PMOS - Fast NMOS (FF), Typical PMOS - Typical NMOS (TT), and Slow PMOS – Slow NMOS (SS) corners. Fig.15 shows the VCO control voltage and the lock detector output for the frequency synthesizer at TT, FF, and SS corners. The locking time is about 2.8 us at TT corner, is about 3.6 us at FF corner, and is 6.1 us at the SS corner. In Fig. 16, the spectrum output of the proposed frequency synthesizer is shown at different corners. Table I gives the reference spur level in different corners.

The phase noise output of the standard and introduced frequency synthesizer is depicted in Fig. 17. The frequency synthesizer phase noise is -108 dBc/HzdBc/Hz at an offset frequency of 200 kHz compared to standard frequency synthesizer phase noise (-112dBc/Hz). Based on the Monte Carlo, simulation, it is verified that by varying the threshold voltage of the devices by 10%, after 50 iterations the phase noise of the introduced frequency synthesizer changes in the range of -107 dBc/Hz to -114 dBc/Hz as is pictured in Fig. 18.

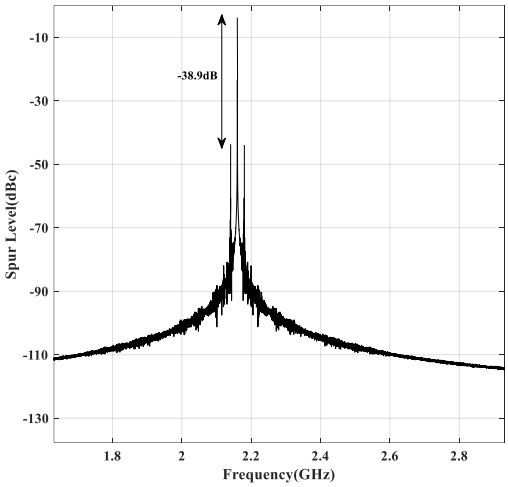

Fig. 13. The output spectrum of the standard frequency synthesizer

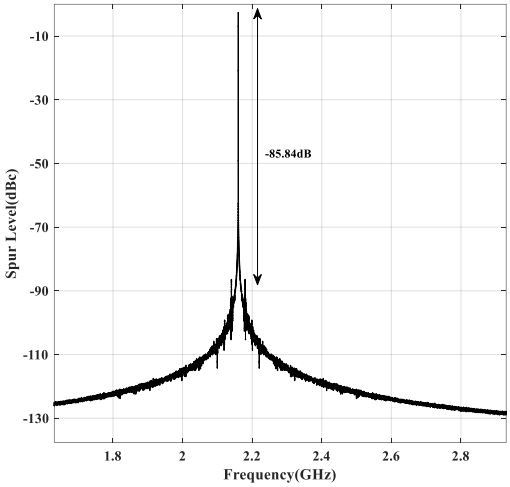

Fig. 14. The output spectrum of the proposed frequency synthesizer

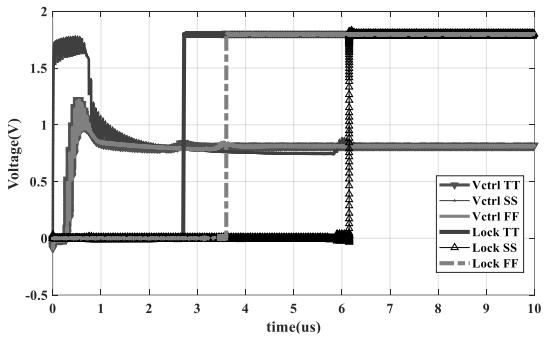

Fig. 15. The VCO control voltage and the lock detector output at different process corners

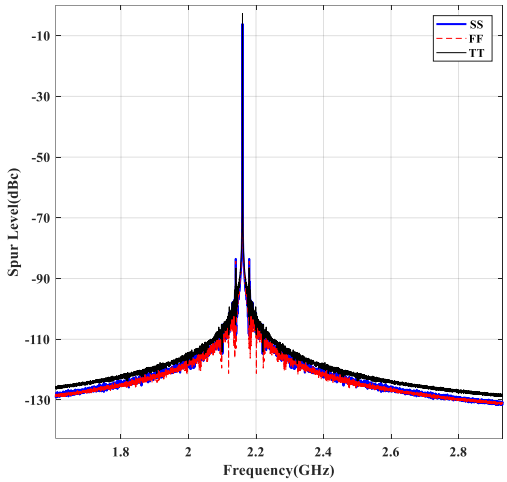

Fig. 16. Reference spur of the frequency synthesizer at different corners

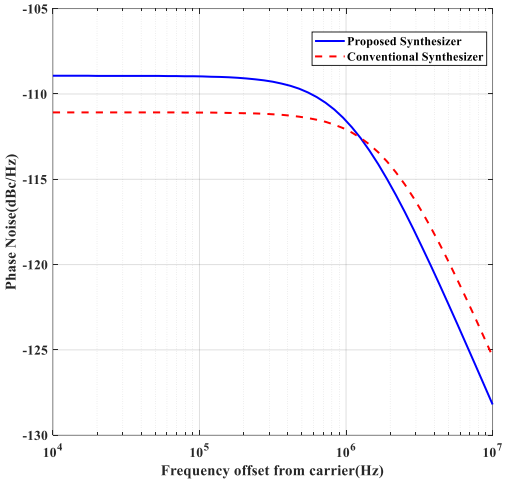

Fig. 17. Phase noise of the standard and introduced frequency synthesizer

Table I. Effect of process corners on the reference spur

Corners	Reference spur(dBc)
TT	-85.84
FF	-81.53
SS	-78.42

The performance data of the introduced frequency synthesizer is listed in Table II compared with low spur frequency synthesizers. The results presented in this paper are the result of the post-layout simulation, but the results listed in Table II for other works are manufacturing results. To compare the spur level of the introduced circuit and other options, a figure of Merit (FOM) was used [28]:

$$FOM\ (dB) = 20\log(\frac{Bandwidth\,(kHz)}{f_{ref}\ (MHz)}) - spur\,(dBc) \qquad (10)$$

The proposed circuit has the smallest reference spur and the best FOM compared to the other options listed in Table II.

4. Conclusion

Through lowering the periodic ripple on VCO control voltage a new frequency synthesizer designed was introduced which yielded a relatively smooth output spectrum and a low reference spur.

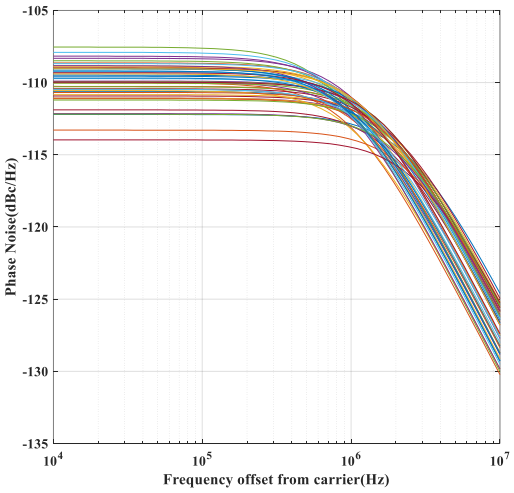

Fig. 18. Monte Carlo simulation for Phase Noise

To show the performance of the new design, the circuit was built using 180-nm CMOS technology and the reference spur was obtained equal to -85.84dBc. in addition, the phase noise was obtained equal to 108dBc/Hz with a 200 kHz offset. In comparison with other studies, the structure introduced here eliminated the reference spur with no need to lower the bandwidth of loop or VCO gain or using a loop filter of higher-order.

Table II. Performance Compared to Previously Published papers

Reference	Technology (nm)	Supply (V)	Output Frequency (GHz)	Reference Frequency (MHz)	K_{VCO} ($\frac{MHz}{V}$)	Spur (dBc)	FOM	Power (mW)	Bandwidth (kHz)	Phase noise (dBc/Hz)
[2]	250	2.5	5.4	10	220	-70	77.95	13.5	25	-63@10KHz
[5]	130	1.5	5.7-6	32.768	45	-68	77.69	3.8	100	-71@100kHz
[11]	65	1.3	81-86	50	2000	-71	91	N/A	500	-80.39@100kHz
[15]	65	1.3	2.05-2.55	50	50	-67	93.02	3.7	1000	-122.8@200kHz
[19]	180	1.8	1.8-3.4	8	N/A	-68/-81	91.5/ 104.5	<18.9	120	<-109@1MHz
[24]	180	1.8	5.18-5.32	20	N/A	<-63	85.9	28.8	280	-102@1MHz
This work*	180	1.8	2.08-2.22	20	200	-85.84	111.8	6.48	400	-108@200kHz

* Post-layout simulation results

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