# An area-efficient broadband balun-LNA-mixer front-end for multi-standard receivers

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**Abstract** An area-efficient wideband receiver front-end for multi-standard receivers is presented. To handle large input signal levels, dual gain modes are employed in the LNA stage. For input signals lower than -17.5 dBm, a noise-canceling balun CG-CS LNA is employed. The LNA features a local feedback loop to reduce power consumption. For input signals in the range of from -17.5 to -5.2 dBm, the CG-CS LNA is bypassed with a balun unit-gain inverter stage. The proposed front-end shows better than -12 dB input matching for both gain modes in the frequency range of 0.4-3.4 GHz. Due to the lack of off-chip balun, the proposed front-end consumes low area. Moreover, the full differential structure leads to enhanced linearity performance. The post-layout simulation results in RF CMOS 0.18 µm process shows the conversion gain of 24.5/13.06 dB in *HG*/*LG* modes. The minimum DSB NF is 3.77/9.84 dB, and the third input intercept point (IIP3) is -7.29/-1.8 dBm. The circuit dissipates 12.93 mW with an active area of 0.073 $mm^2$.

**Keywords:** receiver front-end, balun LNA, low area, noise-canceling, wideband, inductor less.

## 1. Introduction

Nowadays, the emerging of variant wireless communication devices increases the demands for multi-standard receivers. A general representation of multi-standards is to realize the parallel narrowband RF front-ends to support each standard [1]. In other approaches, reconfigurable RF front-ends utilizes narrowband LNAs and mixers, which can be tuned to receive the desired frequency band [2-4]. However, these methods are not efficient in area and power consumption. In a more economical approach, a wideband single RF front-end and mixer are used to cover wide bandwidth. This method leads to a higher level of integration, lower power consumption, and a smaller chip area.

Recently different implementations of wideband receivers are presented [5-10]. The fully differential scheme is more preferred because of the insensitivity to the noise at the supply and ground lines in the LNA stage and the insensitivity to clock feedthrough and noise at the LO port in the mixer stage [8]. However, to benefit the advantages of differential architecture, an off-chip passive balun is required to convert the single-ended signal from antenna to a differential one. The passive baluns degrade the receiver NF, introduces losses and limits the bandwidth [11]. To avoid the passive off-chip balun, an active balun is presented in [12, 13]. Even though the tendency for these active baluns is restricted due to their high power consumption.

This paper presents a broadband low area receiver front-end. In the proposed receiver, an inductor less low power balun common-gate common-source (CG-CS) LNA with the current reused technique is utilized to avoid the need for an off-chip balun in the receiver chain. Interestingly, better noise and linearity performance is achieved in balun LNA with low power consumption. To support large input levels and to avoidance from being saturated for high input levels, the LNA is bypassed with a balun unit-gain inverter stage. This stage generates a signal equal in magnitude but opposite in sign with the RF input signal. Hence, the following mixer stage has differential input signals in both gain modes. The mixer stage is a double-balanced Gilbert cell with a dynamic current injection (DCI) to accomplish low flicker noise. The presented receiver front-end with the BW of 0.4-3.4GHz can be utilized in applications such as digital video broadcasting (DVB) at 450–850 MHz, GSM at 900 and 1800 MHz, Wi-Fi (IEEE802.11b/g/n) and Bluetooth at 2.4GHz, etc.

The paper is organized as follows. In Section 2, the proposed receiver architecture is studied. Simulation results are presented in Section 4, followed by a conclusion.

## 2. Proposed receiver architecture

Fig. **1** presents the architecture of the proposed receiver front-end. The receiver chain includes a Surface Acoustic Wave (SAW) filter to filter out the out of band blockers. The filtered signal is applied to a balun LNA, which is preceded by a low flicker noise mixer. As a multi-standard receiver, the system should have a kind of gain control to handle the large input levels and prevent the system from being saturated. As the bottleneck of the compression point in the receiver chain, the LNA stage consists of two different gain modes.

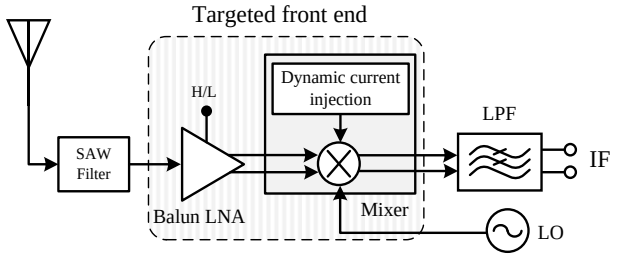



**Fig. 1**. Proposed receiver front-end.

As antennas and RF filters usually produce single-ended signals, single-input LNAs are desired. On the other hand, differential signaling in the receive chain is preferred to decrease second-order distortions. In [12], the balun and the LNA functionality are combined into a single integrated circuit to realize a wideband LNA, shown in figure 2. As shown in this figure, the noise of the $M_{CG}$ appears with the same polarities at output terminals. Thus, satisfying $A_{V,CG}=-A_{V,CS}$, the noise and distortion of the CG transistor can be fully canceled with the CS transistor. However, to lower the noise contribution by the CS stage, this stage should be scaled up n times by admittance scaling ($g_{mCS}=n\times g_{mCG}$, $R_{CS}=R_{CG}/n$).

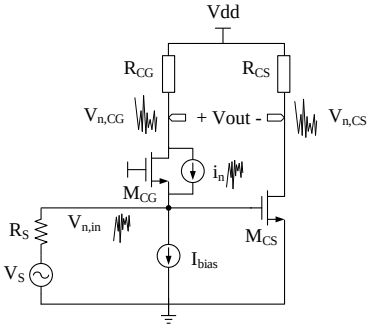



**Fig. 2.** Traditional noise-cancelation balun LNA [12].

To benefit the inherit advances of balun LNAs, the proposed receiver utilizes a balun LNA stage with dual gain modes. The simplified schematic of proposed balun LNA is shown in figure 3. It consists of a low power CG stage for input matching. For small input signals ('*HG*' mode), a CS stage is paralleled with the CG stage to perform the noise-canceling balun LNA. For high input levels ('*LG*' mode), the CS stage turns off not to consume power while the CG stage remains unchanged to perform a termination resistor connected to the input for input matching. To produce differential signals in '*LG*' mode a 'unit-gain inverter stage' is employed in the main signal path to generate output equal in magnitude and opposite in phase with the input signal. This stage should turn off in '*HG*' mode due to power issues.

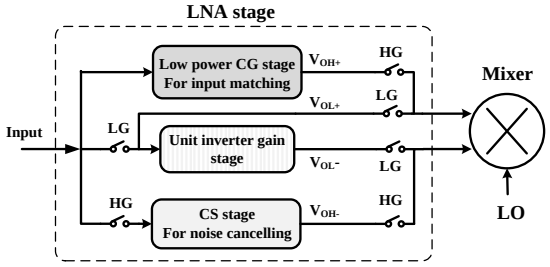



**Fig. 3**. The schematic of proposed balun LNA

Fig. **4** presents the transistor level implementation of the proposed LNA. Load resistors are replaced with active PMOS loads to enhance the gain and the NF performance of the LNA. To determine outputs dc voltage, the $RL_{1,2,3}$ resistors are employed in parallel with PMOS active loads. The paralleled resistors should be large enough in comparison with the output resistance of PMOS transistors, not to degrade the voltage gain. The input matching stage is a CG amplifier to match the input in a wide frequency band. To decrease power consumption a feedback loop is employed around the CG stage to boost the effective input conductance using the transconductance of the tail transistor. The $r_{b1,2,3,4}$ are biasing resistors.

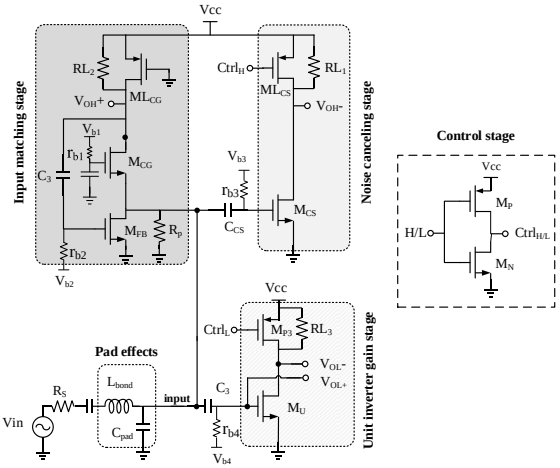



**Fig. 4**. Proposed LNA structure.

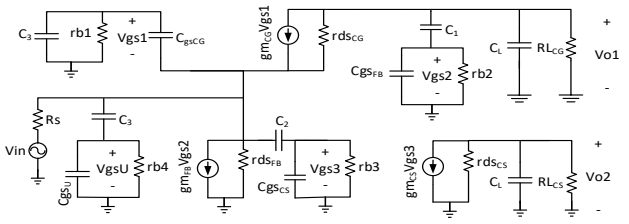



**Fig. 5**. The equivalent circuit model for the proposed LNA.

In *HG* mode (H/L= '1/0', $Ctrl_{H/L}$= '0/1'), the paralleled CS stage cancels the noise and distortions of matching device ($M_{CG}$). Hence, a low power low noise balun LNA is achieved with sufficient gain. To reduce power consumption, in *HG* mode, the unit-gain inverter stage is powered off using a controllable active load.

According to the equivalent circuit model, given in figure 5, the input conductance of the circuit is given by Eq.1. For simplicity, only parasitic gate-source capacitance, transconductance, and the output resistance of the MOS transistors are considered in input matching calculation. The PMOS active loads in the CG, CS, and the unit inverter gain stage are modeled respectively by $RL_{CG}$, $RL_{CS}$, and $R_{P3}$, as they are biased in the triode region.

$$\frac{1}{Rin}=\frac{1}{r_{dsFB}}+\frac{1}{\frac{1}{C_2.S}+(r_{b3}\parallel\frac{1}{C_{gsCS}.S})}+\frac{1}{\frac{1}{C_3.S}+(r_{b4}\parallel\frac{1}{C_{gsU}.S})}+(\frac{1+r_{dsCG}.\left(g_{mCG}+C_{gsCG}.S\right)+Z_L.C_{gsCG}.S}{r_{dsCG}+Z_L})\times\left(1+g_{mFB}.\left(r_{b2}\parallel\frac{1}{C_{gsFB}.S}\right)\times\frac{RL_{CG}}{RL_{CG}+\frac{1}{C_1.S}+\left(r_{b2}\parallel\frac{1}{C_{gsFB}.S}\right)}\right) \quad (1)$$

The first term of Eq. (1) caused by finite CMOS conductance of the $M_{FB}$. The second and third terms are the attenuation of the signal through the CS and the unit inverter gain stages, respectively. These terms are small enough to be ignored compared to the last term. In operating frequency $C_{CS}>>C_{gsCS}$ and $C_3>>C_{gsFB}$ should be satisfied and considering $f>>1/(2\pi\cdot r_{b2}\cdot C_{gsFB})$ and $f>>1/(2\pi.r_{b3}\cdot C_{gsCS})$ in operating frequency, the input conductance and as a result, the input impedance of the proposed LNA is given by:

$$Rin=\frac{1}{g_{mCG}\times(1+g_{mFB}.RL_{CG})} \quad (2)$$

Eq.2 indicates that the proposed matching network reduces the required transconductance of input transistor by a factor of $(1+g_{mFB}\cdot RL_{CG})$. This issue results in input matching with lower power consumption. Besides, a larger scaling factor for the CS stage is achievable for better noise performance.

In *HG* mode the LNA differential gain is:

$$A_{v,diff}=g_{mCG}(r_{dsCG}\parallel RL_{CG})+g_{mCS}(r_{dsCS}\parallel RL_{CS}) \quad (3)$$

For correct noise cancellation, the gain of the CS stage should be equal in magnitude but in opposite sign with the CG stage. So:

$$|A_{v,CG}|=|A_{v,CS}|=g_{mCG}(r_{dsCG}\parallel RL_{CG})=g_{mCS}(r_{dsCS}\parallel RL_{CS}) \quad (4)$$

So, $g_{mCS}=n.g_{mCG}$, the $n.RL_{CS}=RL_{CG}$ should be satisfied to keep output balance.

In noise calculations, the PMOS active loads are modeled with their output resistors as they are biased in the triode region. Furthermore, only thermal noise is studied as the dominant noise source and the flicker noise is not considered for simplicity. The noise factor of the circuit in *HG* mode is calculated as Eq.5.

$$F\approx 1+\frac{\gamma}{\alpha}g_{mFB}.R_S+\frac{\gamma}{\alpha}\times\frac{1}{n.g_{mCG}.R_S}+\frac{1}{n.g_{mCG}{}^2.R_S.RL_{CG}}+\frac{(1+g_{mCG}.R_S)^2}{4\times g_{mCG}{}^2.R_S.RL_{CG}} \quad (5)$$

According to Eq.5, the noise of $M_{CG}$ is fully canceled and the noise of $M_{CS}$ is decreased with a factor of n. To lower the noise distributed by $M_{FB}$, $g_{mFB}$ should be lowered. For this purpose, a large resistor (Rp) is paralleled with $M_{FB}$, shown in figure 4. This resistor provides an auxiliary current path for $I_{MCG}$ and hence reduces the $g_{mFB}$.

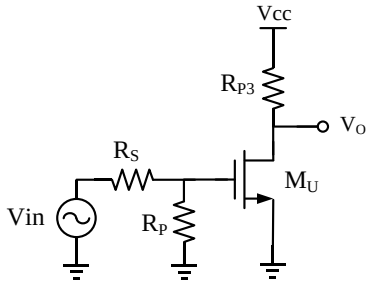



**Fig. 6**. A simplified model for *LG* mode.

In *LG* mode (H/L= '0/1', $Ctrl_{H/L}$= '1/0'), the LNA gain is lowered to mitigates the linearity requirements. In this mode, the CS stage turns off and the CG stage acts as a termination resistor connected to the input for matching ($R_P$). To generate differential inputs for the following double-balanced mixer the input signal is applied to a unit-gain inverter stage to generate a signal with the same magnitude but opposite in sign. According to the simplified model of the LNA in *LG* mode, figure 6, the input matching is:

$$Rin=R_P=\frac{1}{g_{mCG}\times(1+g_{mFB}.RL_{CG})} \quad (6)$$

The noise factor due to the unit-gain inverter stage is computed as:

$$F \approx 1+\frac{R_S}{R_P}+\frac{\gamma.R_S}{g_{mU}.(R_S \parallel R_p)^2}+\frac{R_S}{g_{mU}{}^2.R_{P3}\times(R_S \parallel R_p)^2} \quad (7)$$

For $R_P \approx R_S$, the NF exceeds 3dB. However, as the input level is high in this mode, the signal is less sensitive to noise and linearity is more challenging. Nevertheless, the differential outputs double the gain and lower the NF.

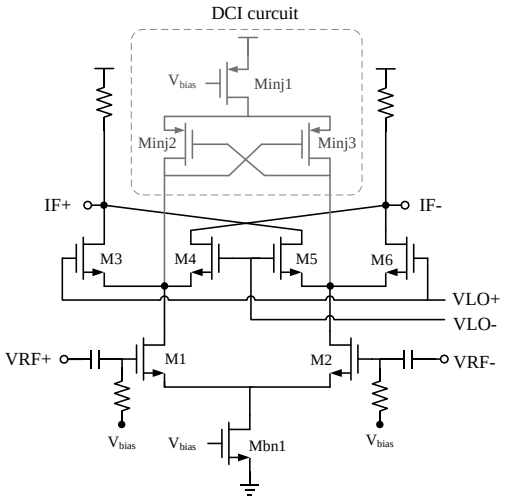



**Fig. 7.** Double-balanced Gilbert type mixer.

In the next stage, the amplified RF signal is applied to a mixer for frequency translation. A double-balanced Gilbert-type mixer is widely used as a downconverter in CMOS receivers, due to high input impedance, the ability to drive low load impedance, good port-to-port isolation and decent gain. However, as the switches are biased at a non-zero drain current, they generate flicker noise. As the gain of the receiver front-end is limited by linearity requirements, the mixer 1/f noise can overwhelm the down-converted small amplitude signal. A current source helper in the RF signal path can improve mixer flicker noise. This approach faces a few drawbacks. First, reducing switches current increase their transconductance. This issue restricts the linearity and BW. Second, current sources increase mixer white noise by injecting their white noise. To overcome these issues, a dynamic current injection is preferred. In [14] a PMOS dynamic switch in serial with an LC tank is employed. The LC tank eliminates the parasitic capacitance and the loading effect of the dynamic switch. However, the LC tank takes a large area. Another approach for dynamic current injection is proposed in [15], figure 7. In this technique, the cross-coupled $M_{inj1,2}$ acts as negative resistance, canceling a part of capacitance at the common source node of switching devices. In addition, dynamic injected current does not add their white noise as they are ON only in switching events.

## 3. simulation results

The proposed direct conversion receiver shown in Fig. **1**, is designed and post-layout simulated in 0.18 µm 1P6M TSMC CMOS process using the Cadence Spectre RF. The layout of the proposed receiver front-end is shown in Fig. **8**, which occupies 0.073 $mm^2$ of the chip area. To make the simulation results more reliable bonding and pad effects are considered as 300 fF capacitance and 1.5 nH inductance. The outputs of balun stages in the time domain are compared in figure 9.

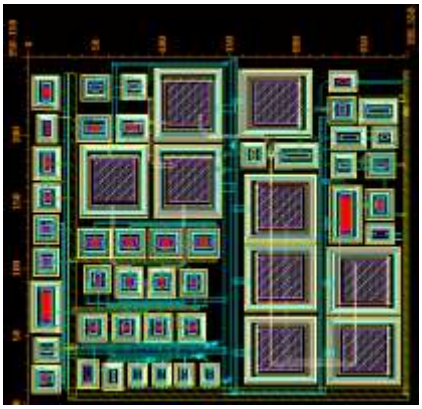


**Fig. 8**.The layout of the proposed receiver front-end.

It should be noted that the output DC voltages are subtracted in simulation results. The input signal level is set to 2 $mV_{P-P}$. The differential output voltage in *HG* mode is 17.44 $mV_{P-P}$ and 4.4 $V_{P-P}$ in *LG* mode. These magnitudes are equal with 18.29 dB and 6.8 dB voltage gain of the balun LNA stage in *HG* and *LG* modes, respectively.

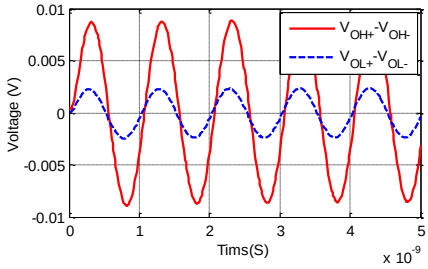



**Fig. 9**. Outputs of balun stages versus time.

Figure 10 presents the conversion gain of the proposed receiver versus input RF frequency and the output frequency is 100 kHz. The maximum gain for *HG* and *LG* modes are 24.5 dB and 13.06 dB, respectively. The BW for *HG* mode is 0.4-3.4 GHz.

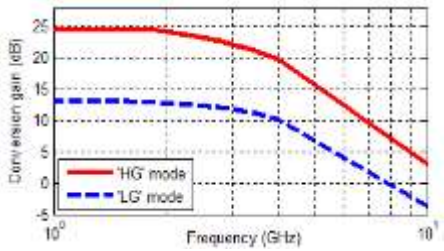



**Fig. 10**. Conversion gain versus input RF frequency ($F_{IF}$=100KHz).

Post-layout simulation results for input impedance matching for both *HG* and *LG* modes are illustrated in figure 11. Simulation results indicate that the receiver shows better than -12 dB input matching in the targeted frequency band.

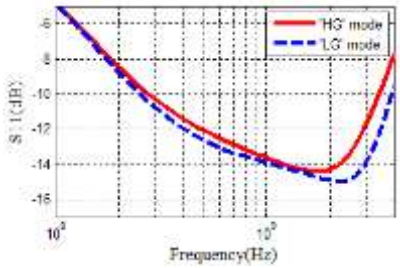
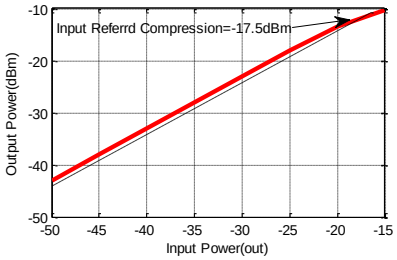
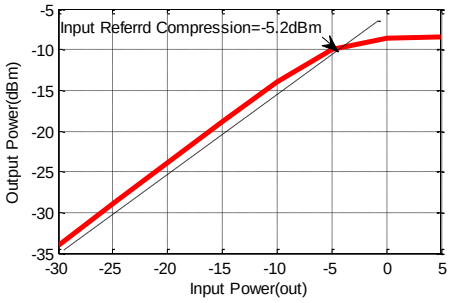



**Fig. 11**. input return loss (S11) versus RF frequency.

The simulations for an input-referred 1dB compression point (P1dB) and the conversion gain of the proposed receiver versus output frequency are shown in figures 12 and 13, respectively. In '*HG*' the maximum allowed input signal level is about -17.5 dBm and the conversion gain is about 22.7 dB. To handle stronger signals, the proposed received presents P1dB of -5.2dBm and the conversion gain of 13.1 dB in the '*LG'* mode. Such large input signals are covered in standards as IEEE 802.11b, GSM, etc.




(a)




(b)

**Fig. 12**. Simulated P1dB ($f_{LO}$=2.4GHz, $f_{IF}$=100MHz). (a) *HG*, (b) *LG*.

The NF post-layout simulation result is given in figure 14. The NF in *HG* mode is 3.77 dB with the 1/f noise corner frequency (fc) of about 60 kHz. Reducing the gain with 9.6 dB, the noise rises to 9.87 dB. It should be noticed that the *LG* mode is active for the input signals with a large magnitude, which are less sensitive to noise.

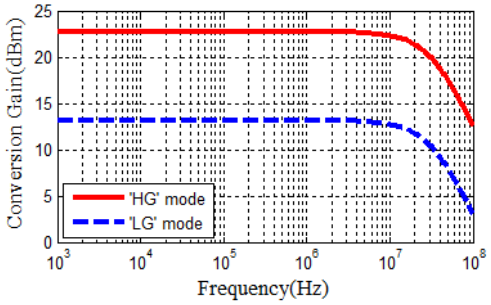



**Fig. 13.** Conversion gain versus output frequency.

Post-layout two-tone IIP3 simulation results with 100 MHz offset around the center frequency for *HG* and *LG* modes are demonstrated in figure 15. The IIP3 is -7.29 dBm for *HG* mode while it increases to -1.8 dBm in *LG* mode.

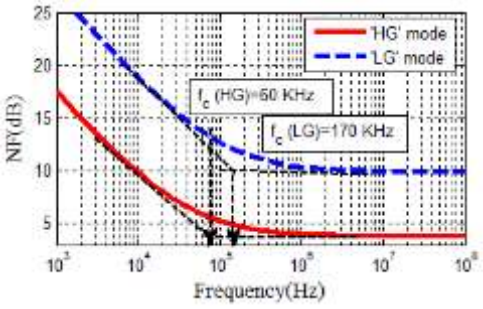
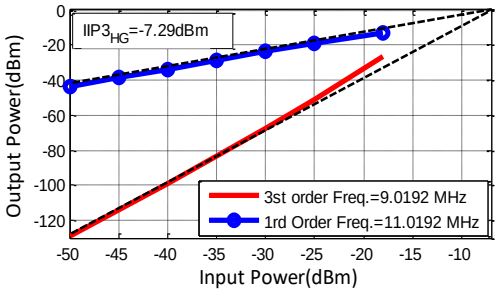
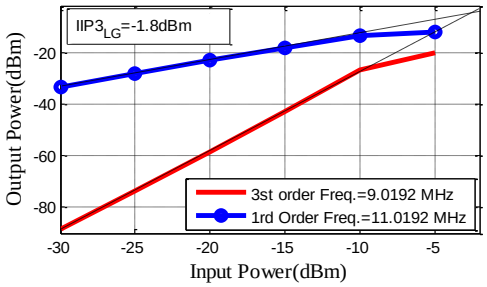


Figure 14. NF versus output frequency.




(a)




(b)

**Fig. 15.** IIP3, post-layout simulation result. (a) *HG*, (b) *LG*.

**Table 1.** Performance comparison with recent works

| | This work | | [16] | [7][a] | [17] | [18][a] | | |
|---|---|---|---|---|---|---|---|---|
| Technology (nm) | 180 | | 180 | 130 | 180 | 130 | | |
| Frequency (GHz) | 0.4-3.4 | | 2-4.5 | 1-5.5 | 2.4 | 2.4 | | |
| Conversion Gain(dB) | 13.06 | 24.5 | 28.9 | 17.5 | 18.2 | 44 | 29 | 12 |
| DSB NF (dB) | 9.84 | 3.77 | 3.3 | 3.9 | 10 | 3.75 | 14 | 30 |
| IIP3 (dBm) | -1.8 | -7.29 | -17.8 | +0.84 | -18.8 | -31 | -16 | 0 |
| Power (mW) | 12.93 | | 17.8 | 34.5 | 5.57 | 25.2 | | |
| Chip area ($mm^2$) | 0.073 | | NA | 0.315 | 2.08 | 0.612 | | |

[a] measurement results

Figure 16 sketches the proposed front-end specification in gain, NF and IIP3 for different input levels. For input signal levels smaller than -17.5 dBm, the proposed receiver shows a voltage gain of 24.5 dB in *HG* mode with the NF of 3.77dB and the IIP3 of -7.29 dBm. However, for larger input signals, ranging from -17.5 to -5.2 dBm, the proposed structure is set to LG mode with a gain of 13.06 dB. This prevents the system from being saturated. In this mode, the NF is 9.87dB with the linearity of -1.8 dBm.

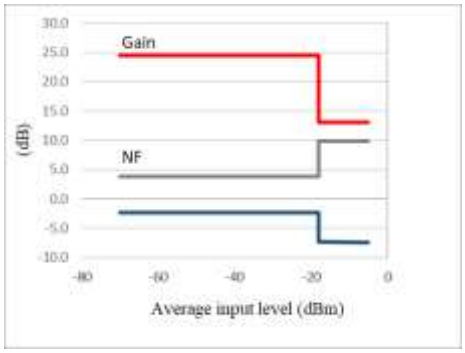



**Fig. 16.** The specifications of the proposed receiver front-end

The performance comparison of the proposed receiver with recently reported works is given in Table 2. Although power is not as low as [17], the proposed receiver achieves better linearity and noise performance in a wide frequency band. [7] presents broad bandwidth with enhanced linearity, however, the power is tripled. In [18], for a step of 15 dB in gain, IIP3 and NF degrade approximately 16 dBm and 14 dB, respectively. Whereas, the proposed receiver presents 4.9 dBm and 6 dB variation in IIP3 and NF, for a 9.5 dB gain step. Ref [16] archives better voltage gain and consequently smaller NF at the expense of dramatically degrading Linearity and power consumption. The chip area in the proposed receiver, with a large difference, is the smallest compared to other references. Such an efficient area can significantly lower the cost.

The performance of the proposed receiver is summarized in Table 2, with the portion of consumed power in each part.

## 4. Conclusion:

An inductor less, area-efficient receiver front-end is presented with the BW of 0.4-3.4GHz. To mitigate the need for an off-chip balun a modified CG-CS balun LNA is employed. The balun LNA utilizes the current reused technique to achieve low power, low noise, and low area structure. To endure higher input levels, CG-CS LNA is

bypassed with a balun unit-gain inverter stage to generate differential outputs for the proceeding mixer stage. The full differential structure improves the receiver linearity performance. The mixer stage is a Gilbert cell exploiting dynamic current injection to reduce the flicker noise. The performance analysis in common with post-layout simulation results confirms that the proposed front-end presents an admirable performance in BW, noise and linearity performance while takes a smaller area.

**Table 2.** Summary of receiver performance

| **Receiver front-end** | ***LG*** | ***HG*** |
|---|---|---|
| **Conversion gain (dB)** | 13.06 | 24.5 |
| **Noise figure (DSB)** | 9.87 | 3.77 |
| **IIP3 (dBm)** | -1.8 | -7.29 |
| **IIP2(dBm)** | 77.08 | 77.95 |
| **ICP (dBm)** | -6.3 | -17.4 |
| **Input insertion loss (dB)** | -14.8 | -14.2 |
| **Power consumption(mW)** | Total 12.93<br>LNA<br>CG stage 0.93<br>CS stage 4.8<br>Unit gain inverter stage 2.55<br>Mixer 7.2 | |
| **technology** | 180 nm | |

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