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A Low-Ripple High-Voltage Power Supply for Photomultiplier Tubes

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Abstract
Photomultiplier tubes (PMTs) require a stable, low-ripple high-voltage power supply with stringent load regulation and line regulation criteria. This paper introduces an innovative high-voltage power supply capable of converting a 220V AC input voltage into a DC output voltage that can be adjusted from -100V to -3kV. In the event of an arc or short circuit, the output voltage abruptly reduces to limit the output current to its rated value of 5mA. This system employs both linear and switching converters to yield a consistently smooth output voltage with voltage ripple as low as 400mV. The switching converter utilizes a push-pull converter while the linear converter meticulously regulates the output voltage. The paper outlines design considerations for the appropriate selection of components. Simulation results validate the performance of this proposed power supply under a variety of conditions, including input voltage and reference voltage variations, abrupt load changes, and short-circuit scenarios. Furthermore, experimental results from a fabricated prototype confirm the functionality of this high-voltage power supply for PMT applications.

Keywords
High Voltage, Low Ripple, Power Supply, Photomultiplier, Accurate, Load Regulation, Line Regulation, Short Circuit Protected.

1. Introduction

Photomultiplier tubes (PMTs) are versatile devices with a wide range of applications, including but not limited to particle detection [1], cosmic gamma-ray research [2], particle accelerators [3], aerosol scattering detection, oil well logging, neutrino experiments, and oil well monitoring [4].

PMTs demand high-performance High Voltage Power Supplies (HVPS) capable of delivering kilovolts with minimal voltage ripple. In these applications, the output voltage ripple is a critical factor as it directly impacts system accuracy and performance. For instance, in laser Doppler anemometry applications where PMTs convert light signals into photocurrent signals, a stabilized PMT power supply at the 0.1% level is essential. It should also allow for external regulation of the output voltage within a range of 0.5 to 3 kV [5]. Consequently, fluctuations in input voltage and load changes should have a negligible impact on the power supply's output voltage.

Furthermore, beyond their use in PMTs, HVPSs find numerous applications in various industries and research fields. These applications include insulation testing, materials processing, water disinfection, welding, tomography, particle accelerators, electron microscopes, X-ray systems, precipitation and filtering, electrostatic painting, and communication [6]-[13].

In [14], a resonant HVPS with zero voltage switching (ZVS) is introduced for use with micro-channel plate photomultiplier tubes. This power supply features a transformer with multiple secondary windings, allowing precise regulation of the output voltage.

A high step-up DC-DC converter for renewable energy systems, combining active-network and coupled inductors to achieve ultra-high voltage gain at low duty cycles is introduced in [15]. Compared to counterparts, the design doubles the gain for identical duty cycles and turns ratios while reducing switch voltage stress to less than half.

In [16] a novel transformerless DC-DC boost converter with ultra-high voltage gain is proposed. Modular extension enhances gain and reduces switch stress. The design employs switched inductor/capacitor circuits with unified PWM control. Inductor currents and capacitor voltages remain balanced across all operating modes, eliminating the need for multiple sensors.

Ref. [17] presents a HVPS that incorporates a ceramic transformer in place of the traditional magnetic transformer. The ceramic transformer is constructed from a ceramic bar and utilizes the piezoelectric effect to generate high voltage. While the exact ripple magnitude is not specified, it notes that the ripple is proportional to the load current, thereby limiting the load current supplied to the photomultiplier.

In [18], a circuit for a voltage multiplier is proposed, capable of generating 2kV from a 12V input for a PMT dynode system. This high-voltage power supply maintains the linearity of PMT gain even with anode-pulse heights reaching up to 100 mA.

A multichannel high voltage system is introduced in [19], employing an active Cockcroft-Walton type voltage

Table I. Specifications of Various High Voltage Power Supplies.

Reference	Input Voltage	Output Voltage (kV)	Rated Current (mA)	Ripple (mV)	Line Regulation (%)	Load Regulation (%)
[5]	12~16 VDC	0.5~3	2	240	--	--
[14]	10 VDC	-0.2~-3	3	6000	0.2	0.35
[17]	15 VDC	1.5~2.5	0.12	--	--	--
[18]	12 VDC	0.8~2	--	2.5	--	--
[19]	55 VDC	0~-2.1	0.19	200	--	--
[20]	10~120 VDC	-1.6~-2.4	0.15	9500	--	--
[21]	12 VDC	1.5	1	33	--	--
[22]	40 VDC	2	0.8	100	--	0.1
[23]	--	15	15000	7500	--	--
CC228-01Y	12 VDC	-0.2~-1.25	0.5	30	0.01	0.01
CC228-01Y	16 VDC	-2~-10	0.2	100	0.1	0.1
Proposed HVPS	220 VAC	-0.1~-3	5	400	0.03	0.03

multiplier directly connected to each PMT. Similarly, reference [20] presents a HVPS designed for PMT applications, utilizing a Cockcroft-Walton voltage multiplier instead of a transformer. It notes that increasing the error amplifier gain can reduce steady-state error but may negatively affect efficiency and stability margins.

In [21], a non-dissipative voltage divider is introduced, which is based on a forward converter and a multi-winding transformer. Each secondary voltage is rectified and filtered to eliminate voltage ripple. This design can generate a 1.5kV output voltage from a 12V input voltage through a regulator circuit, ensuring that the output voltage of the HVPS remains at the desired level.

An economical, robust and reliable multi-channel power supply system for the CMS hadronic forward calorimeter PMTs is developed in [22] which is based on a custom power supply module, containing three clusters of three HV outputs.

In [23], a very low-ripple high voltage high-power DC power supply is proposed for vacuum tube applications. This power supply utilizes a series linear regulator in conjunction with a high-frequency high-power DC interleaved converter. The ripple level is significantly reduced in the first stage by increasing the ripple frequency, and further reduction is achieved using the linear regulator in the second stage.

Some studies mitigate output voltage ripple by enlarging the output capacitor. While effective, this method increases both cost and system size while also elevating short-circuit current levels during fault conditions. Although a crowbar circuit (implemented across the load) can limit fault currents [24,25], this approach compromises power supply reliability.

Alternative approaches [26,27] increase the switching frequency to reduce output capacitance requirements compared to the first method. However, this technique necessitates a substantial frequency increase, leading to higher switching losses and control complexity.

The third approach employs active ripple elimination techniques, which can target either Low-frequency (2ω) ripple cancellation for rectified AC voltages [28], or High-frequency switching ripple suppression [23,29]. This method actively injects compensating signals rather than relying solely on passive filtering.

A review of various high-accuracy HVPS systems in terms of input voltage, output voltage, output current, maximum ripple, as well as line and load regulation is summarized in Table I.

This paper introduces a highly stable and precise HVPS with the ability to generate -100V ~ -3kV from 220VAC input voltage. The output voltage ripple of the proposed HVPS is as low as 400mV under rated conditions. The circuit is equipped with current protection mechanisms to restrict the current in the case of short circuit or arcing. It exhibits a maximum output voltage variation of 0.03% in the case of 10% fluctuation in input voltage (line regulation) or a change in load from no-load to full load (load regulation).

The remaining of the paper is structured as follows: Section II introduces the circuit of the proposed HVPS. Design considerations are investigated in Section III. The simulation and experimental results are presented in Section IV and section V, respectively. Finally, Section VI concludes the paper.

2. The Proposed Circuit

The block diagram of the proposed HVPS is depicted in Fig. 1, designed to convert 220V AC from the power grid

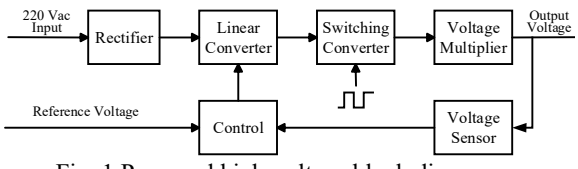

Fig. 1 Proposed high-voltage block diagram.

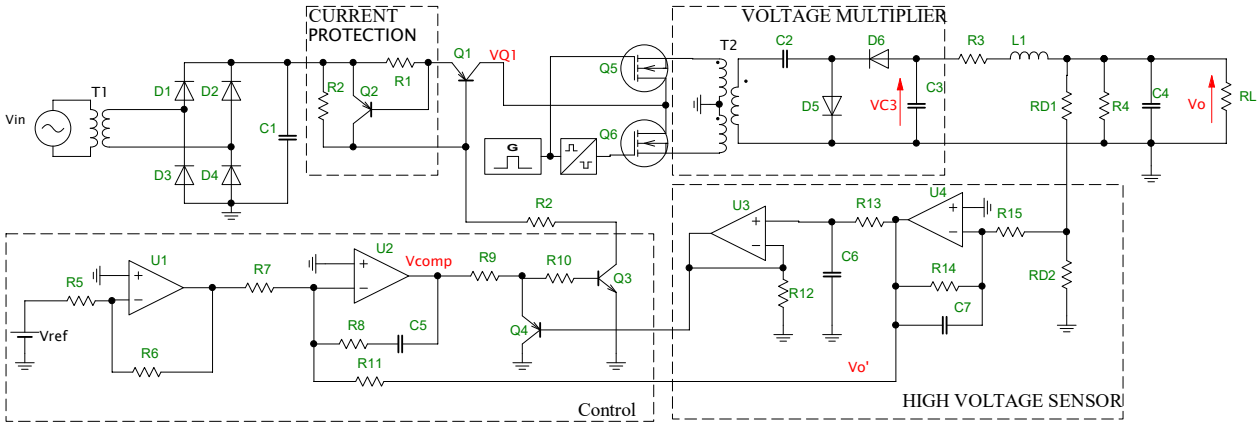

Fig. 2. The proposed high voltage power supply.

into a variable high DC voltage. The circuit comprises several essential components, including rectifier, linear converter, switching converter, voltage multiplier, high-voltage sensor, and control section.

The 220V grid voltage is stepped down and rectified using a rectifier. This rectified voltage is then applied to a linear converter which regulates the output voltage by applying an appropriate voltage to a switching converter. The switching converter consists of a push-pull converter and a high-voltage high-frequency transformer to boost the voltage. A Cockcroft-Walton voltage multiplier is employed to double the amplitude of the push-pull voltage. A voltage sensor is implemented to scale the output voltage down to a level that can be easily measured or monitored. The control section handles the linear converter by incorporating a proportional-integral (PI) controller and continually comparing the output voltage with a predefined reference value.

The detailed circuit of the proposed high-voltage power supply is shown in Fig. 2. The input voltage is stepped down to a suitable level for the linear regulator using transformer T_1. It is then rectified by a diode bridge comprising diodes D_1 to D_4 and subsequently filtered by capacitor C_1. The applied voltage to the switching converter continuously adjusting through transistor Q1, which functions as the linear regulator. The switching converter comprises MOSFETs Q_5 and Q_6 and a high-voltage high-frequency transformer, T_2. The output voltage of the push-pull transformer is ultimately rectified and doubled using a Cockcroft-Walton voltage multiplier, incorporating capacitors C_2 and C_3 along with diodes D_5 and D_6.

Three mechanisms have been incorporated to limit the potential short-circuit current. The first mechanism utilizes resistor R_1 and transistor Q_2 as a current protection circuit, which reduces the applied push-pull voltage in the event of a short-circuit occurrence. The second protection circuit utilizes transistor Q_4. In the event of a short circuit, the output voltage collapses to zero, activating Q_4. This action interrupts the current flow through Q_3 and Q_1, preventing any output voltage from appearing at the linear regulator. Finally, resistor R_3 and inductor L_1 serve as output current-limiting components.

A second-order filter, comprised of inductor L_1 and capacitor C_4, is employed to reduce the voltage ripple at the output terminals. R_L represents the photomultiplier tube equivalent resistor.

The high output voltage is first scaled down using R_{D1} and R_{D2} and measured using a high voltage sensor, which includes components R_{14}, R_{15}, C_7, and op-amp U_4. This measured voltage is then filtered through a low-pass filter, which consists of R_{13} and C_6, and subsequently buffered by components R_{12} and op-amp U_3.

In the control section, the measured output voltage is compared with a reference value, V_{ref}. A compensating voltage, V_{comp}, is generated using a proportional-integral (PI) controller consisting of components R_8, C_5, and U_2. This voltage adjusts the linear regulator output which consequently handles the applied voltage of the push-pull converter. Transistor Q_4 is employed to ensure a soft and controlled power supply turn-on.

3. Small Signal Analysis

To derive the transfer function of the proposed circuit, the current protection circuitry (comprising R_2 and Q_2) and the soft-start section (comprising Q_4 and U_3) are omitted. The small-signal block diagram of the proposed circuit is illustrated in Fig. 3.

The voltage at the output of the controller, V_{comp}, can be expressed as:

$$Vcomp = \frac{Z_1}{R_7}\left(\frac{R_6}{R_5}Vref - \frac{R_7}{R_{11}}Vo'\right) \quad (1)$$

where $Z_1 = R_8 \| 1/sC_5$ and Vo' represents the measured output voltage. Thus $G_1(s)$ can be expressed as follows:

$$G_1(s) = \frac{Z_1}{R_7} = G_0\frac{1+s/s_{wz1}}{s} \quad (2)$$

where $G_0 = 1/R_7C_5$ and $s_{wz1} = 1/R_8C_5$ represent static gain and zero of $G_1(s)$, respectively.

The small signal model of transistors Q_1 and Q_3 based on the hybrid-π model is show in Fig. 4. Z_2 represents the impedance seen at the input of the push-pull converter. The following relationship can be established by considering that the base current of Q_1 is supplied by the collector current of Q_3:

$$i_{B1} = \beta_3 i_{B3} \tag{3}$$

Therefor $G_2(s)$ can be expressed as:

$$G_2(s) = \frac{V_{Q1}}{V_{comp}} = \frac{Z_2\beta_1 i_{B_1}}{(r_{\pi_3} + R_{910})i_{B_3}} = \frac{Z_2\beta_1\beta_3}{(r_{\pi_3} + R_{910})} \tag{4}$$

where β_1 and β_3 represent the current gains of transistors Q_1 and Q_3 and R_{910} denotes the series combination of R_9 and R_{10} (i.e. $R_{910} = R_9 + R_{10}$).

The small signal model of the voltage doubler circuit is shown in Fig. 5 where Z_3 represent the load and filter impedance and n donates the turn ratio of transformer T_2.

During DT_s (where T_s is the switching period and D is the duty cycle of switch Q_5), when Q_5 is turned on and Q_6 is turned off, the current passing through capacitors C_2 and C_3 can be expressed as:

$$i_{C_2} = \frac{\beta_1 i_{B_1}}{n} \tag{5}$$

$$i_{C3} = -\frac{V_{C_3}}{Z_3} \tag{6}$$

During $D'T_s$ when Q_5 is turned off and Q_6 is turned on, the following currents become:

$$i_{C_2} = -\frac{\beta_1 i_{B_1}}{n} \tag{7}$$

$$i_{C3} = \frac{\beta_1 i_{B_1}}{n} - \frac{V_{C_3}}{Z_3} \tag{8}$$

In steady-state conditions, the average current through the capacitors over one switching period must be equal to zero. By averaging the current through capacitor C_2 over one switching period, we obtain:

$$D\left(\frac{\beta_1 i_{B_1}}{n}\right) + D'\left(-\frac{\beta_1 i_{B_1}}{n}\right) = 0 \tag{9}$$

Thus, the on-time and off-time durations in one switching period must be equal, as given by:

$$D = D' = 0.5 \tag{10}$$

Similarly, by averaging the current through capacitor C_3 over one switching period, the following equation is obtained:

$$D\left(-\frac{V_{C_3}}{Z_3}\right) + D'\left(\frac{\beta_1 i_{B_1}}{n} - \frac{V_{C_3}}{Z_3}\right) = 0 \tag{11}$$

By substituting (10) into (11), we have:

$$\frac{\beta_1 i_{B_1}}{2n} = \frac{V_{C_3}}{Z_3} \Rightarrow V_{C_3} = \frac{Z_3\beta_1 i_{B_1}}{2n} \tag{12}$$

Consequently, the expression for $G_3(s)$ is derived as:

$$G_3(s) = \frac{V_{C_3}}{V_{Q_1}} = \frac{V_{C_3}}{\beta_1 i_{B_1} Z_2} = \frac{Z_3}{2nZ_2} \tag{13}$$

The output filter model, $G_4(s)$, can be expressed as:

$$G_4(s) = \frac{V_O}{V_{C_3}} = \frac{R_4 \| 1/sC_4}{Z_3} = \frac{R_4}{Z_3}\frac{1}{1 + s/w_{p4}} \tag{14}$$

where $w_{p4} = 1/R_4C_4$ represents the pole location of $G_4(s)$.

The transfer function of the measurement section, $H(s)$, can be written as:

$$\frac{Vo'}{Vo} = -\frac{R_{D2} \| R_{15}}{(R_{D2} \| R_{15}) + R_{D1}}\frac{R_{14} \| 1/sC_7}{R_{15} + (R_{D1} \| R_{D2})} \tag{15}$$

Given that $R_{D1} \gg R_{D2}$ and $R_{D1} \gg R_{15}$, equation (15) can be approximated by:

$$H(s) = -\frac{H_0}{1 + s/w_{p0}} \tag{16}$$

where $H_0 = \frac{R_{D2}R_{14}}{R_{D1}(R_{15} + R_{D2})}$ and $w_{p0} = 1/R_{14}C_7$ represent static gain and pole of $H(s)$, respectively.

Referring to Fig. 3, the open loop gain can be expressed as:

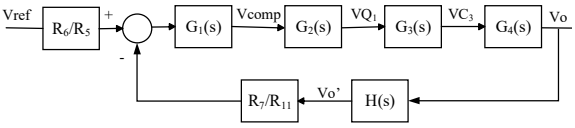

Fig. 3 The small signal block diagram of the proposed circuit.

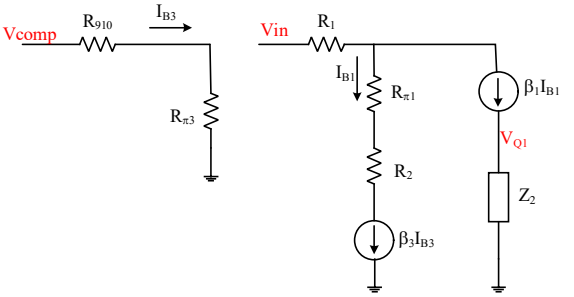

Fig. 4 Small signal model of transistors Q_1 and Q_3.

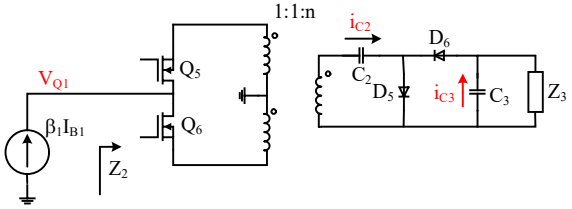

Fig. 5 Small signal model of the voltage doubler circuit

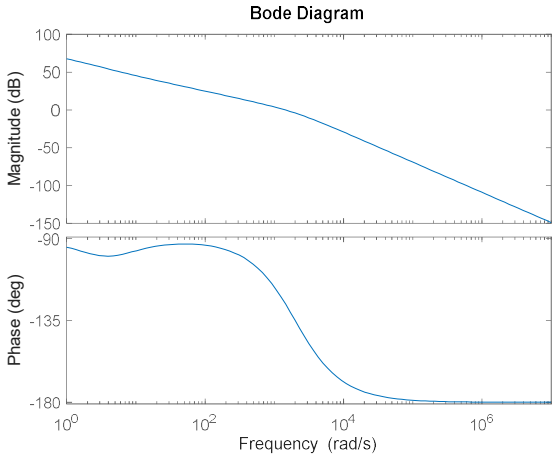

Fig. 6 Bode plot of the system.

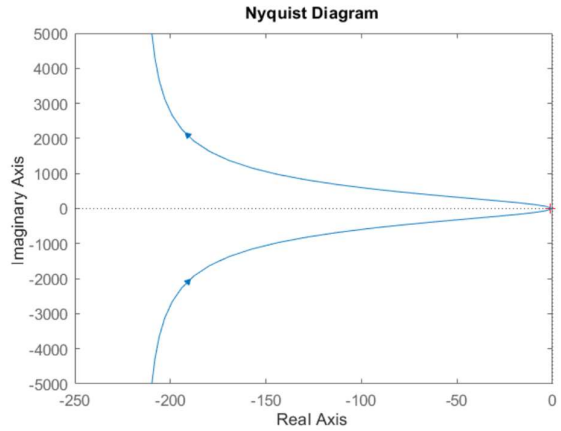

Fig. 7 The system Nyquist plot.

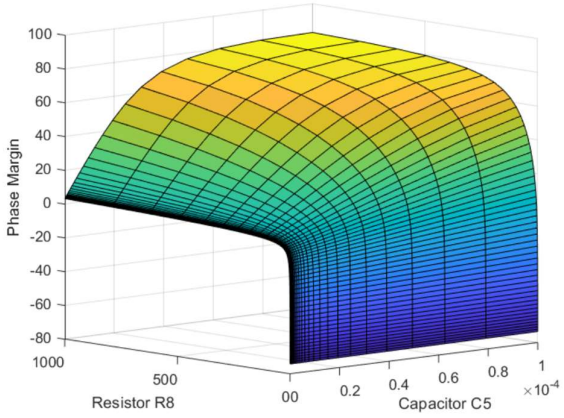

Fig. 8 Phase margin variation due to control parameters.

$$T_{OL}(s)=\frac{G_0H_0\beta_1\beta_3R_4R_7}{2nR_{11}(r_{\pi_3}+R_{910})}\frac{(1+s/s_{wz1})}{s(1+s/w_{p0})(1+s/w_{p4})} \quad (17)$$

and the resulting closed-loop transfer function is obtained by:

$$T_{CL}(s)=\frac{V_0}{V_{ref}}=\frac{R_6R_{11}}{R_5R_7}\frac{T_{OL}(s)/H(s)}{1+T_{OL}(s)} \quad (18)$$

4. Design Considerations

The specifications of the proposed power supply are detailed in Table 2. The nominal values for the output

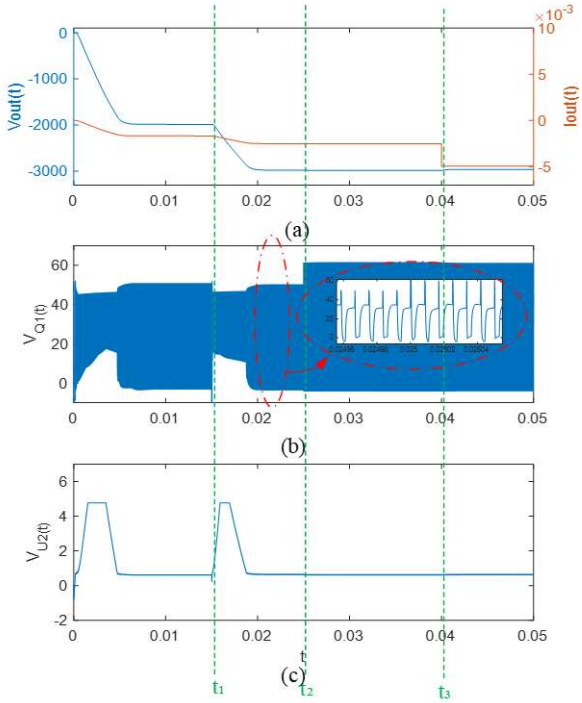

Fig. 9. Simulation voltage and current waveforms; (a) Voltage and current of the output terminals; (b) Voltage of the linear regulator, V_{Q1} (c) Voltage of the compensator, V_{comp}.

voltage (V_{out}) and output current (I_{out}) are -3kV and 5mA, respectively. The output voltage ripple is constrained to a maximum of 400 mV. Both line regulation and load regulation should be limited to 0.03%.

Considering the maximum grid voltage fluctuation to be 10%, the minimum voltage across the filter capacitor, C_1, can be approximated as:

$$V_{C_1,\min}\simeq 0.9V_m-\frac{I_{Q_1}}{2C_1f_{ac}} \quad (19)$$

Where V_m represents the voltage amplitude at the secondary winding of transformer T_1, and f_{ac} denotes the grid frequency. I_{Q1}, the collector current of transistor Q_1, is proportional to the load current (I_{out}) and can be derived as follows:

$$I_{Q_1}=2nI_{out} \quad (20)$$

Combining (19) and (20) yields:

$$V_{C_1,\min}\simeq 0.9V_m-\frac{nI_{out}}{C_1f_{ac}} \quad (21)$$

For proper operation of the linear regulator, Q_1 must remain in active mode, requiring its emitter voltage to exceed its collector voltage. This condition is expressed by the inequality:

$$0.9V_m-\frac{nI_{out}}{C_1f_{ac}}-R_1I_{out}>\frac{V_{out}}{2n} \quad (22)$$

The majority of power losses in the power supply occur in the linear regulator, with transistor Q_1 being the primary

contributor. To minimize this loss, the voltage V_m should be kept as low as possible. When the grid voltage drops by 10%, the voltage across Q_1 is assumed to be 20% of V_m to ensure proper operation of the linear regulator in all conditions. Thus, by neglection voltage drop on R_1, we have:

$$0.9V_m - \frac{V_{out}}{2n} = 0.2V_m \Rightarrow V_m = \frac{5V_{out}}{7n} \quad (23)$$

By substituting (23) into (22), neglecting R_1 and choosing $C_1 = 4700$ µF, the upper limit of n is determined to be 141. The lower limit of n can be derived based on the V_m constraint, as introduced in Equation (23). In the proposed circuit, the turn ratio of transformer T_1 is selected as 5, resulting in $V_m = 61$ V. Accordingly, the lower limit of n is determined to be 35. Therefore, transformer T_2 shall be designed with a turns ratio n satisfying $35 < n < 141$.

Under normal operating conditions the voltage across R_1 must remain below the Q_2's turn on threshold voltage to keep the current protection circuit disabled, as specified by:

$$2nR_1I_{out} < V_{\text{threshold}} \quad (24)$$

The voltage ripple across the capacitor C_3 is equal to:

$$\delta V_{C_3} = \frac{I_{out}}{2f_S C_3} \quad (25)$$

where f_s represents the push-pull switching frequency. assuming $R_L << R_4$ and neglecting R_{D1} and R_{D2}, the output voltage ripple can be expressed as:

$$V_{ripple} = \frac{I_{out}/2f_sC_3}{s^2(L_1C_4) + s(R_3C_4 + \frac{L_1}{R_L}) + (1 + \frac{R_3}{R_L})} \quad (26)$$

Resistor R_3 serves as a current-limiting element designed to ensure the short-circuit current never exceeds the specified maximum I_{SC}

$$R_3 = \frac{V_{out}}{I_{SC}} \quad (27)$$

The key parameters of the proposed circuit are listed in Table 3. By selecting the PI controller parameters as R_8=10kΩ and C_5=22µF, and applying (17), the Bode plot of the system is obtained as shown in Fig. 6. It can be seen that the system has infinite gain margin and 45° phase margin, indicating that it is robust and stable. The Nyquist plot, shown in Fig. 7, confirms the stability of the system across all frequencies. The power supply controller should respond quickly, eliminate steady-state error, and track the reference voltage without introducing oscillations. R_8 and C_5 are the primary components of the PI controller, and variations in their values directly affect the transfer function $G_1(s)$. While adjusting the PI controller parameters within the range 10mΩ $< R_8 <$ 1kΩ and 1nF $< C_5 <$ 1µF, the system maintains an infinite gain margin. However, the phase margin will vary depending on these settings as shown in Fig. 8. R_8 is associated with the proportional part of the controller, while C_5 corresponds to its integral part. As observed, the proportional part of this controller contributes more significantly to system instability compared to the integral part.

The losses of MOSFETs are the sum of conduction losses and switching losses, as expressed in the following equation:

$$P_{Loss_{Q5}} = P_{Loss_{Q6}} = \frac{1}{2}R_{DS(on)}(I_D)^2 + \frac{1}{2}V_{DS}I_D(t_{on} + t_{off})f_s \quad (28)$$

where $R_{DS(on)}$, t_{on}, and t_{off} are MOSFET on-resistance, rise time, and fall time, respectively. Since $R_{DS(on)}$ is very low in MOSFETs, conduction losses are often negligible compared to the switching losses. Thus, losses associate with switches Q_5 and Q_6 can be approximated as:

$$P_{Loss_{Q5}} + P_{Loss_{Q6}} \simeq 2(t_{on} + t_{off})f_sP_{out} \quad (29)$$

Under worst-case conditions, when the grid voltage increases by 10%, the power dissipation in Q_1 can be calculated as:

$$P_{Loss_{Q1}} = (1.1 \times V_m - R_1I_{out} - V_{out}/2n)2nI_{out} \quad (30)$$

By neglecting R_1 and substituting (23) into (30), the power losses of the linear regulator can be determined as:

$$P_{Loss_{Q1}} = \frac{4}{7}P_{out} \quad (31)$$

Since power losses in Q_1, Q_5, and Q_6 constitute the dominant portion of total circuit losses, the system efficiency can be approximated as follows:

$$\eta = \frac{7}{11 + 14(t_{on} + t_{off})f_s} \quad (32)$$

5. Simulation Results

To confirm the operation and functionality of the proposed HVPS, a simulation was conducted using MATLAB/Simulink software. The outcomes of this simulation are presented in Fig. 9.

The circuit is powered on at t=0, with half of the nominal load connected to the output terminals. In this scenario, the reference voltage is set to -2kV, and the grid voltage is maintained at 90% of the nominal value. It is observed that the output voltage rapidly converges to the reference voltage within a brief 6ms timeframe.

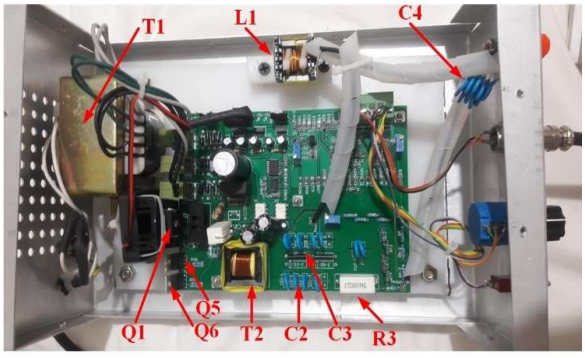

Fig. 10. Experiment prototype of the proposed HVPS.

During this interval, the control circuit consistently compares the output voltage with the reference voltage to generate a compensating signal. By reaching the output voltage to the reference value, the compensating voltage, V_{comp}, decreases. This compensating voltage adjusts the linear regulator to provide an adequate voltage for the push-pull converter, as can be seen in Fig. 9(b).

At $t=t_1$, the reference voltage is increased to -3kV, causing both the compensating voltage and the average voltage of the linear regulator to rise in order to adapt to the new conditions. The grid voltage is increased to 110% of its nominal value at $t=t_2$. It can be seen the output voltage remains unaffected by grid voltage variations.

At $t=t_3$, a nominal load is connected to the output terminals, causing an increase in the output current. Notably, the output voltage initially drops by 20V, but this decrease is subsequently compensated by the control circuit within 30ms.

6. Experimental Results

The proposed HVPS has been designed and fabricated, as depicted in Fig. 10. The output voltage can be adjusted from -100V to -3kV by modifying the reference voltage through a multiturn volume. the power supply ensures that the output voltage ripple does not exceed 400mV even at full load. It takes a 220V AC input voltage and reduces it to 40V AC using transformer T_1.

Inductor L_1 and capacitor C_4 form a low-pass filter to reduce the high-frequency ripple voltage, moreover, L_1 limits the current slope in the event of short-circuit conditions. Additionally, a high-power resistor, R_3, is integrated to restrict short-circuit currents. The output voltage ripple should not exceed 400mV in the situation of ±10% input voltage fluctuation or load variation from no load to full load.

Fig. 11 displays the output voltage of the power supply (Ch.1), the compensator voltage, V_{comp} (Ch.3), and the collector voltage of transistor Q_1 (Ch.4). At the initial stage, the output terminals are short-circuited, and the output voltage remains at zero until t=80ms. During this period, the compensator voltage is at the maximum value while the voltage of the linear regulator is forced to zero due to the presence of the current protection circuit, comprising R_1 and Q_2.

At t=80ms, the short circuit is resolved, and the output voltage quickly stabilizes at -2.2kV within 10ms. By closely examining the output voltage in more detail, the ripple amplitude is found to be ±100mV, and it oscillates at twice the switching frequency. Under normal operating conditions, the compensator voltage varies in such a way as to establish the output voltage at the desired value.

The output terminals experience a second short circuit condition at t=290ms. As observed, the compensator voltage suddenly drops to zero. However, the output voltage gradually decreases to zero, due to the energy stored in the voltage multiplier capacitors, C_2 and C_3.

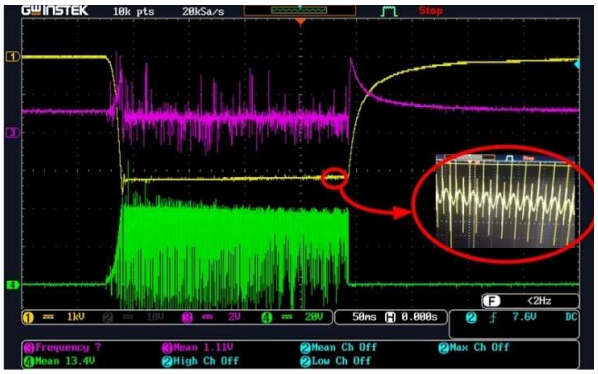

Fig. 11. Experimental waveforms; Ch.1 is the output voltage, Ch.3 is voltage of compensator, V_{comp}, and Ch.4 is voltage of linear regulator, Q_1.

Fig. 12. Experimental waveforms; Ch.1 is the output voltage, Ch.2 is push-pull gate voltage, Ch.3 is voltage of compensator, V_{comp}, and Ch.4 is voltage of linear regulator, Q_1.

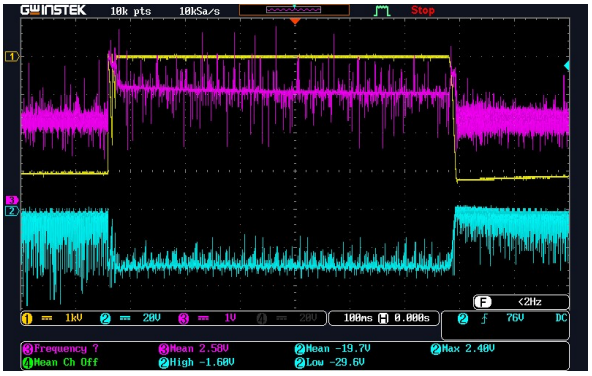

Fig. 13. Experimental waveforms; Ch.1 is the output voltage, Ch.2 is collector-emitter voltage of the linear regulator, Q_1, and Ch.3 is the voltage of current protection resistor, R_1.

Fig. 12 provides a detailed view of the gate voltage of the push-pull inverter, the compensator voltage, and the output voltage of the linear regulator under normal conditions, when the output voltage is set to its nominal value, -3kV. The gate signals for the push-pull transistors, Q_5 and Q_6, are complementary and operate at 90kHz.

To achieve a high-bandwidth controller and effectively regulate the output voltage while adhering to the maximum allowable ripple, no filters should be installed

at the output of the compensator circuit and the linear regulator. Consequently, the regulator's output voltage decreases at twice the switching frequency, leading to switching losses that impact the power supply's efficiency.

Fig. 13 illustrates the voltage at the output terminal, the collector-emitter voltage of the linear regulator transistor, Q_1, and the voltage across the current protection resistor, R_1, under both normal conditions and during a short circuit event.

Under normal conditions, when operating at the rated voltage of -3kV and the rated current of 5mA, the voltage across R_1 remains at 2V, which is low enough not affecting operation of the linear regulator. However, when a short circuit occurs at the output terminals at t=160ms, the voltage across R_1 increases to 3V. This voltage increment can turn Q_2 on and subsequently reduce the base current of the linear regulator transistor, Q_1. As a result, voltage of the push-pull inverter drops to zero.

7. Conclusion

This paper proposed a high-voltage power supply system that provides a promising solution for applications requiring precise and stable high-voltage supplies, such as photomultiplier tubes (PMTs). It has the ability to quickly respond to load variations, input voltage fluctuations, and short-circuit events. The control circuit, which utilizes a proportional-integral (PI) controller, effectively regulates the output voltage while keeping the voltage ripple within an allowable range. Experimental results from the prototype confirm functionality of the circuit in the case of normal and short circuit conditions.

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