Tabriz Journal of Electrical Engineering (TJEE), vol. 55, no. 1, 2025 Serial no. 111
DOI: 10.22034/tjee.2024.60668.4812

A Low-Power, Area-Efficient ADC-Direct Artifact-Tolerant Neural Recording System Using Digital Block Sharing

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Received: 20/02/2024, Revised: 03/07/2024, Accepted: 07/09/2024.

Abstract
This article presents a front-end block for recording neural signals of the direct Analog-to-Digital Converter(ADC) type based on the continuous-time Delta-Sigma Modulator (CT-DSM) to reduce power consumption and occupied space. The system works as a CT-DSM with a single-bit quantizer in the artifact-free state. When the artifact is present, the DSM is saturated, which is detected by the digital block, and the second feedback path estimates the amplitude of the artifact. By reducing the amplitude of the artifact from the input signal, the system can convert the neural signal when the artifact is present. The process of designing and implementing the proposed circuit is based on three general ideas of improved circuit design of the block with the highest power consumption, using a 7-bit counter to detect the saturation of the DSM and sharing the digital part. The implementation of the transistor level in CMOS technology is TSMC 0.18um with a channel area of 0.013mm^2 and power consumption of 4.6uW.

Keywords
Neural recording, Neural front-end, Low-area, Low-power, Delta sigma modulator, DSM.

1. Introduction

Various neurological and psychological disorders can be diagnosed and treated clinically using special electronic tools to detect and stimulate neural signals. Studies have shown that the symptoms of abnormal brain activity can be reduced through electrical stimulation of the brain's neural signals. When this is done in a closed loop, the effectiveness of such treatment is significantly improved. For example, Deep Brain Stimulation (DBS) has been used successfully to reduce motor effects in patients who have Parkinson's disease[1, 2]. Existing stimulation methods rely on continuous current open-loop stimulation. The article [3] shows a microsystem designed for high-density neural recording utilizing 256 channels and incorporating delta compression with 3D electrodes.

The primary objective of this system is to enhance the efficiency of neural activity recording and data transmission by reducing the overall data volume. Each recording channel comprises two stages of ac-coupled amplification: the first stage exhibits a gain of 34 dB, while the second stage features a programmable gain. The output signal is subsequently sampled and stored using a switched-capacitor sample-and-hold circuit. The delta compression technique is applied by calculating the difference between two consecutive samples and discarding values below a predefined threshold.

The system is constructed using 0.35um CMOS technology, achieving a bandwidth of 5kHz, power consumption of 15 uW, and occupying a space of 0.04 mm^2.

The study [4] presents a compact neural recording front-end featuring a two-stage delta-sigma incremental ADC with 120 mVpp offset compensation. The system has been implemented using 180nm CMOS technology with 10khz bandwidth and occupies 0.0046 mm^2 of space for 14.6uW power consumption. A two-stage incremental delta-sigma ADC increases the accuracy and resolution of neural recordings, while a 120mVpp offset compensation feature minimizes offset errors to improve signal integrity. This front-end design strikes a remarkable balance between small and high performance, making it suitable for integrating with miniature neural recording devices.

A versatile 64-channel neural recording system-on-chip (SoC) with system activity-dependent data throughput is presented in [5]. The SoC is designed to adapt its processing and data transfer rates based on neural activity levels, ensuring efficient data management and minimizing power consumption. This innovative approach allows the system to dynamically adjust its throughput in response to detected neural activity, optimizing data transfer and storage capabilities. The system uses 0.35um CMOS technology, which occupies 0.3 mm^2 space per channel and requires an average power consumption of 110 uW, including all analog, digital, and memory parts.

In [6], a 128-channel wireless neural recording integrated circuit (IC) with a power consumption of 6 mW is presented. This IC has advanced spike feature extraction capabilities that allow accurate identification and analysis of neural spikes. The 128-channel recording circuit

included eight 16-channel analog front-ends, a digital signal processor for spike detection, feature extraction, and ultra-wideband (UWB) telemetry. Time-division multiplexing is used for all 16 channels to share an ADC. A low power consumption of 6 mW makes this IC suitable for implantable neural recording applications where energy efficiency is critical. A 2.4 GHz Ultra-Low-Power Reconfigurable Asymmetric Transceiver is presented in [7], designed for a single-chip wireless neural recording integrated circuit. The 2.4GHz transceiver architecture offers flexibility and efficiency in wireless neural signal transmission and reception.

However, changes in neural behavior during stimulation amplitude resetting can lead to a loss of treatment effectiveness and harmful side effects. Closed-loop stimulation is a desirable foundation in advancing clinical neuroscience, where stimulation parameters are adapted in real-time using feedback from recorded neural signals. In this regard, the design and construction of ICs for closed-loop neural modulation systems have been actively researched[8, 9]. The implantable two-way neural interface system with low energy consumption is used for patients who need closed-loop control of brain and neural functions for a long time[10]. One of the essential parts of this system is the front end of the neural signal recording circuit, which requires a more complex design and construction for this front end due to simultaneous recording with stimulation[11].

Signal recording inside the body using implantable electrodes is the most effective method for direct control of prosthetic devices and treatment of neurological diseases. In this method, electrodes can be placed directly on the brain's surface or inside the brain to record electrical activity from the cortex or inside the brain. Brain signals presented with this method have a better Signal-to-Noise and Distortion Ratio (SNDR) but are more sensitive to artifacts. In addition, these signals have high spatial and temporal resolution. The signals extracted from these methods have a frequency of several mHz to 10 kHz, and their range is 10uV to 10 mV. Fig. 1 shows the frequency range required to record neural signals and their signal range. As shown in Fig. 1, the minimum SNDR value required to record neural signals with artifacts is at least 80 dB[12-16].

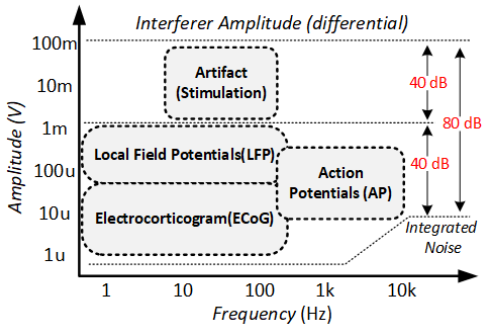

Fig. 1. Amplitude and frequency bio-signal characteristics in the neural signal recording.

2. Neural recorder architecture

A problem with conventional two-way neural interface systems is that it is difficult to accurately record neural signals and electrical stimulation simultaneously. Electrical stimulation is often controlled in flow mode due to irregular tissue-electrode impedance[17, 18].In such microsystems, due to the high voltage (i.e., usually higher than 10 V) of the applied electrical stimulation pulse, large Stimulation Artifacts (SA) with an amplitude of hundreds of millivolts are generated to interfere with the recorded neural signals. Given that neural signals are typically very weak and have amplitudes as small as a few microvolts, recording neural signals in the presence of large SA is not straightforward. When using conventional neural recording circuits consisting of a high-gain Instrumentation Amplifier (IA) and a low Dynamic Range (DR) ADC, SA easily saturate the Front-End IA, resulting in poor performance. become nervous (Fig. 2(a)). A simple approach is not to record the signal when artifacts are present. Short-time gating may not cause excessive loss of recorded signal information for a microsystem with a single excitation channel. However, if the microsystem has several excitation and recording channels, the loss of information becomes unacceptably high.

Another recently proposed approach is implementing an adaptive filter circuit for each pair of recording and stimulation channels to actively remove SA (Fig. 2(b)). If fewer recording and stimulation channels and their possible combinations become too large, the overhead to remove the active artifact becomes too high. New designs using low-gain IA followed by a high-DR ADC have been proposed to overcome the limitations of conventional high-gain IA recording architectures (Fig. 2(c)). IA saturation is avoided in this new structure, and the overall circuitry has a small enough distortion to maintain the accuracy required to record small-amplitude neural signals with large-amplitude artifacts.

Another approach is to use a direct conversion structure, which does not use any front-end gain layer, to use the high DR-ADC (Fig. 2(d)). Although this structure is freed from the IA saturation problem, the ADC should have a large enough DR (more than 80 dB) while consuming low power[19, 20].

A recent new construction removes the artifact at the output of the first transconductance stage (Gm) using a secondary feedback path (artifact Digital-to-Analog Converters (DAC)) (Fig. 2(e))[21, 22]. In this method, after detecting the modulator's instability due to the artifact's presence by a digital block, the second DAC is activated and increases or decreases the approximate value of the artifact at the input of the modulator from the original signal. This work stabilizes the CT-DSM with the first DAC, and the system can record the neural signal in the presence of the artifact. The advantage of this system is that there is no need for a large DR of the DSM with the main DAC, so it is possible to use the degree modulator designed as a required system.

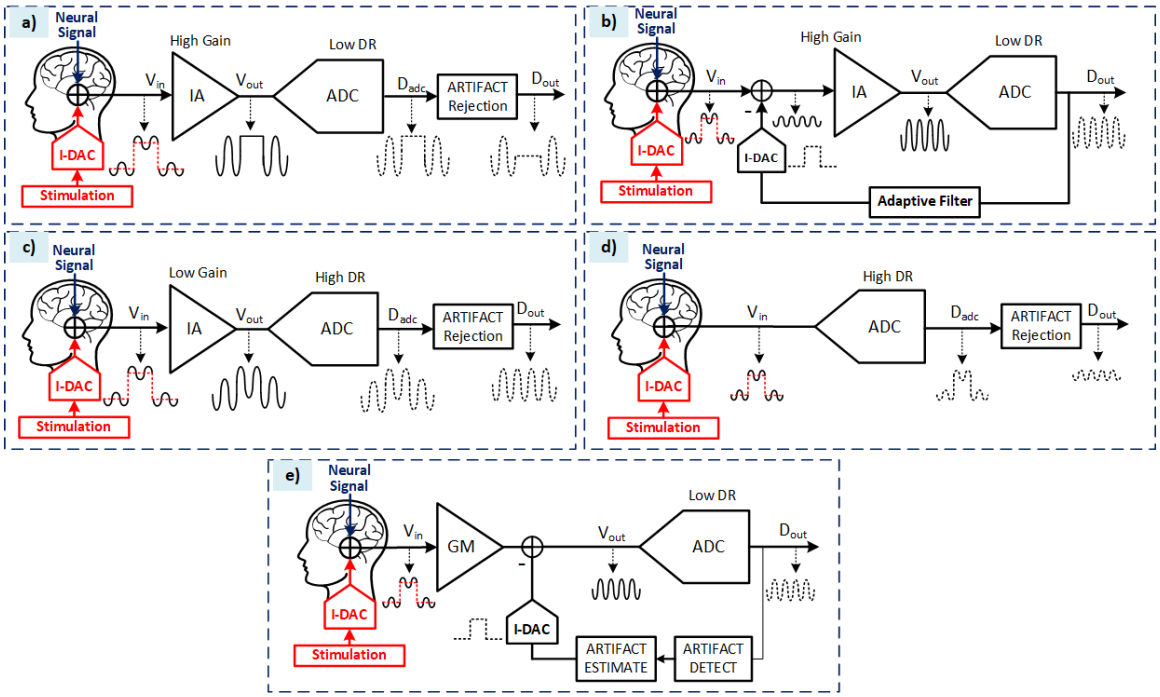

Fig. 2. Different front-end structures and DM stimulation artifact mitigation techniques. (a) A conventional structure, (b) Adaptive filter-based artifact canceller;(c) a saturation-free structure with a low-gain IA and a high-DR ADC, (d) High DR CTDSM without an IA, (e): ADC-Direct Artifact-Tolerant based artifact canceller.

3. Design of the ADC structure for recording neural signals

By reviewing the structures presented in the articles of the last few years[9, 14, 15, 17, 20, 23-28], the parameters of Table I can be reached regarding the requirements of the front end for neural signal recording. These parameters show the minimum requirements of a neural signal recorder. Considering the implantable component of closed-loop neural signal recording systems, the two components of power consumption and occupied area are of particular importance in increasing the efficiency of these systems. Improving the two mentioned components makes reaching systems with a longer lifespan and more channels possible. Therefore, this article seeks to improve these two components in the selected structure, and suggestions are made to reduce the power and occupied area with the minimum observance of other parameters.

Table I. Neural Front-End System Requirements Summary.

Parameter	Range
Power / Channel	<10uW
Area / Channel	<0.05 mm^2
Differential Artifact Tolerance	>100 mVpp
DR	> 80 dB
SNDR	> 40 dB
Bandwidth	1 Hz ~ 500 Hz (LFP) 500 Hz ~ 5kHz (AP)
Input-Referred Noise (IRN)	< 10-μV_{RMS}
DC Input Impedance	>100MΩ
Electrode Differential Offset	≥±50 mV

3.1. Selected structure

Fig. 3 presents a first-order CT-DSM (with two feedback paths and artifact detection and artifact size estimation blocks) in[21]. In this structure, due to the elimination of the system input artifact in the output of the first transconductance, it is possible to eliminate the AC coupling capacitors; as a result, using the chopper stabilizer does not destroy the input resistance. This issue makes auxiliary circuits not used compared to other designs, and the system's overall performance improves.
The chosen architecture uses two 1-bit current-mode DAC(IDAC) ("Main" IDAC for regular operation and "artifact" IDAC for times when artifacts are present). The system's function is that when there is no artifact in the first step, the CT-DSM only performs the signal conversion with an input transconductance, a one-bit quantizer, and the "main" IDAC. If the artifact occurs, the system of the first stage will become unstable and produce consecutive zeros or ones in its output.
The artifact approximation section and the "artifact" IDAC are activated by detecting the saturation of the CT-DSM (by the saturation detection digital block) (second step). Then, in the third step, the "main" IDAC is turned off, and the larger loop of the system performs the approximation of the artifact domain. This estimate is later used to compensate for the DM artifact while quantizing the neural signal. Then, after approximating the artifact domain, the "main" IDAC is added to the system, and the CT-DSM converts the neural signal (fourth step).
The current generated by the "artifact" IDAC counteracts the large current coming from the GM stage due to offset/artifact. In contrast, the "Main" IDAC current quantizes the output current of the Gm stage corresponding to the input neural signal.

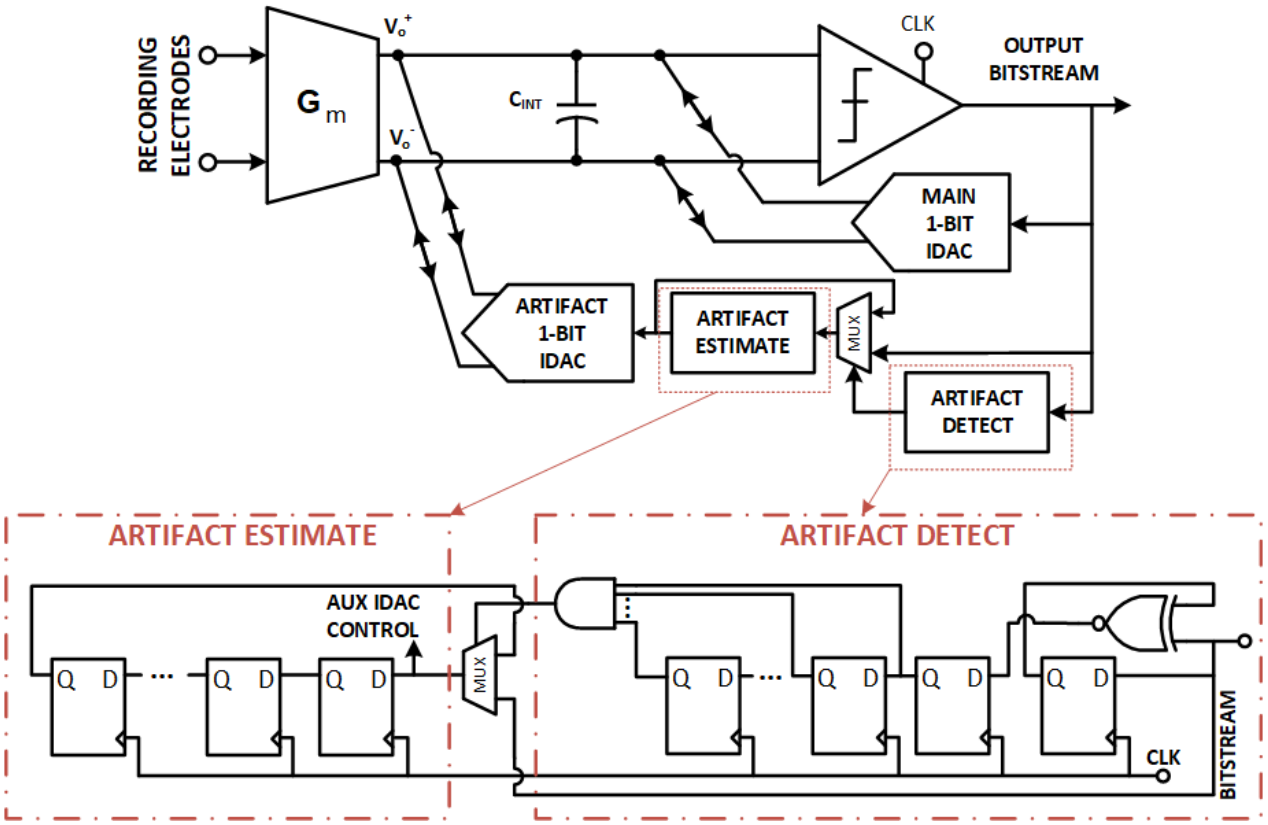

Fig. 3. Architecture of DC-coupled ADC-direct artifact-tolerant neural recording channel as presented in [21].

Post-layout simulation results of neural recording channel architecture based on the CT-DSM proposed in [21] show that the DR value is equal to 90.9dB, the power consumption of the whole system is 5.4uW (3.53uW corresponds to the input Gm layer). Its occupied area is 0.035 mm^2 (more than 70% of the area occupied by the digital part). Although the designed system has been able to meet the requirements in terms of the parameters of Table 1, there are two fundamental problems in the design and implementation of the system. The first case is related to the consumption power of 65% Gm of the total consumption power of the system. The second issue is that a small channel area with high scalability is achieved thanks to the simple architecture, circuit reuse, and minimal use of passives (a 2pF integration capacitor).
However, using 100 registers and 100 inputs NAND in the saturation detection block and 100 registers in the artifact domain approximation makes up more than 70% of the system's digital circuits occupied. In this article, the proposed system has a better efficiency in terms of system power consumption and occupied area due to the two mentioned cases. Therefore, three stages of optimized design have been worked on the selected system, which will be discussed further.

3.2. Step1: GM input, Quantizer and DAC design

3.2.1 Input Gm structure

As shown in Fig. 4, a rail-to-rail folded-cascode architecture is adopted for the transconductance amplifier. To further improve linearity, both tail current sources of the input pair use the cascade structure. A transconductance amplifier with desired specifications is designed in 0.18um technology and simulated in a spectra/Cadence environment. The gain of the transconductance amplifier is 47dB, GBW is equal to 40kHz, and the phase margin is 89.8 degrees for the power consumption of 2.7uW.

3.2.2 Quantizer and DAC

In Fig. 5, the implemented circuit of the main IDAC is shown. The 1-bit current-mode DAC must be designed to push/pull a constant current into the integrated capacitor of the Gm-C filter to form the Δ part of the ΔΣ modulator. As shown in Fig. 5, a simple push/pull charge pump is used for this block. It should also be noted that any mismatch between the push and pull currents becomes an offset error and will not affect the dynamic performance of the ADC ΔΣ[21]. The "Artifact" IDAC structure is the same as the "Main" IDAC, and only the pressure/tension constant current is different.
Fig. 6 shows the circuit structure of the quantizer implementation. A StrongArm comparator is used in the initial part of the quantizer. This comparator triggers an SR-Latch to create an entirely logical level to trigger the DAC. The comparator minimizes the overall power consumption thanks to its fully dynamic operation (i.e., no static power). Therefore, the power consumption of the quantizer is equal to 1.5uW.

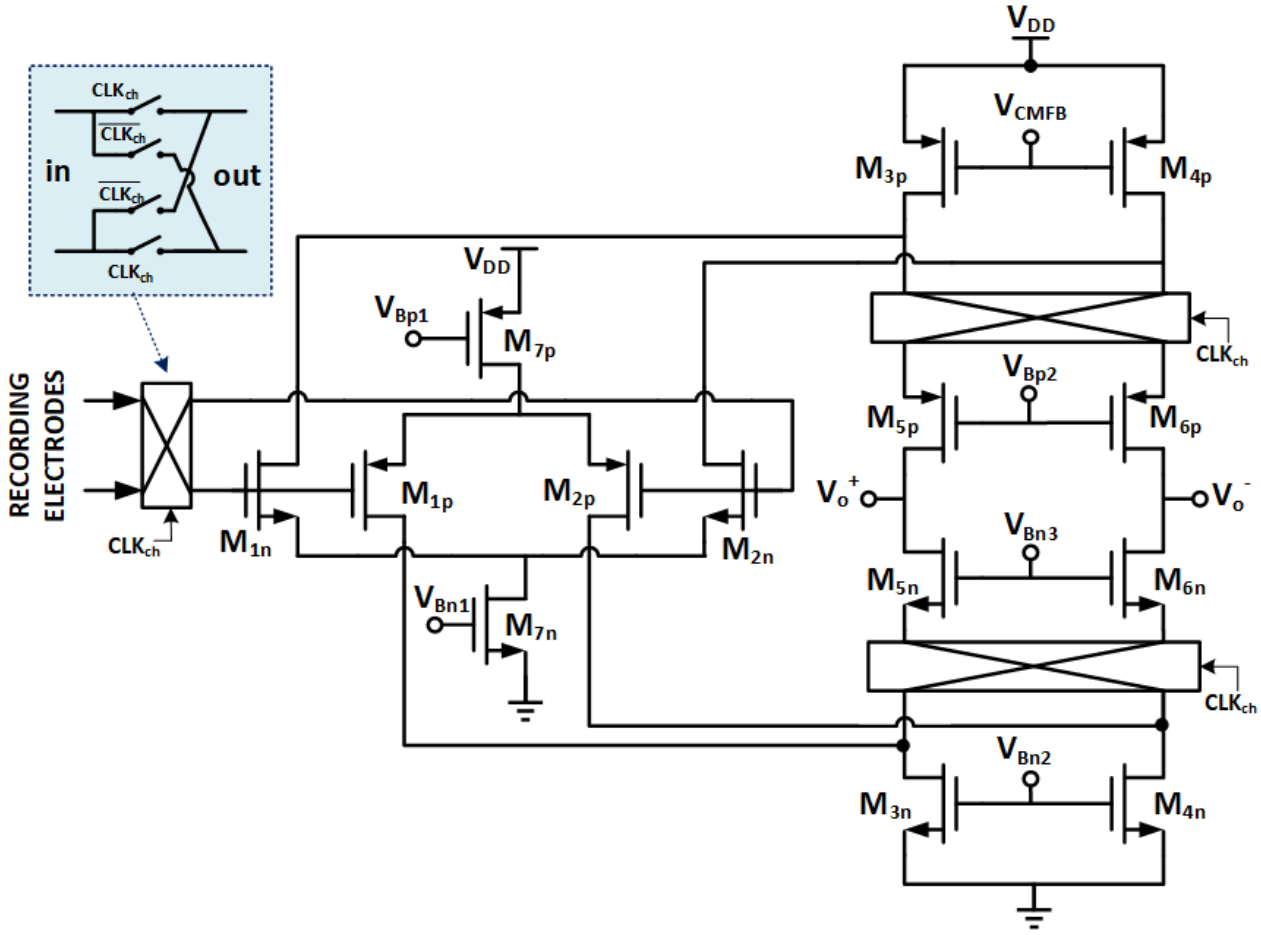

Fig. 4. Circuit structure of the transconductance amplifier.

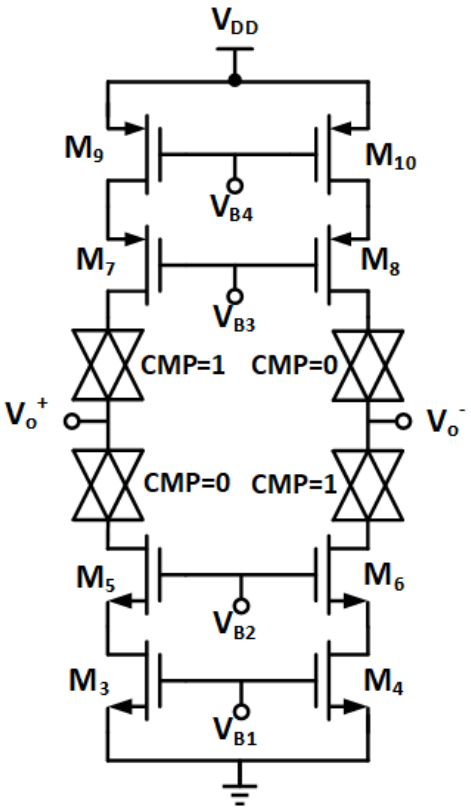

Fig 5. Transistor level implementation circuit of the IDAC.

3.2.3 Chopping technique

Flicker noise is one of the most critical factors affecting the converter's accuracy in medical signal recording systems with low frequencies. The standard solution to this problem is the Chapping technique[29]. The main idea of this technique is to separate the signal frequency band and the noise frequency band. In the first stage, the input signal is modulated to a higher frequency through a chopper, and then the modulated signal with offset noise and flicker passes through the circuit. The offset and flicker noise is in the low-frequency band, and the modulated signal is in the high-frequency band, so the offset and flicker noise do not affect the signal. Finally, a chopper modulates the input signal passed through the amplifier to the baseband.

3.3. Step2: Suggests using a 7-bit counter to detect the presence of artifacts

Using 100 registers + 100 NAND inputs in the saturation detection block in the implementation circuit [21] is the main factor in increasing the occupied area of the chip. The proposed circuit for implementing the saturation detection block in the proposed system is shown in Fig. 7. Using a 7-bit counter using JK-DFF and multiple NANDs can do the same thing as 100+ NAND registers with about 60% less footprint. Fig. 8 shows the placement of the implementation of the single-channel neural signal recording system using a 7-bit counter, the occupied area of which is equal to 0.028 mm^2.

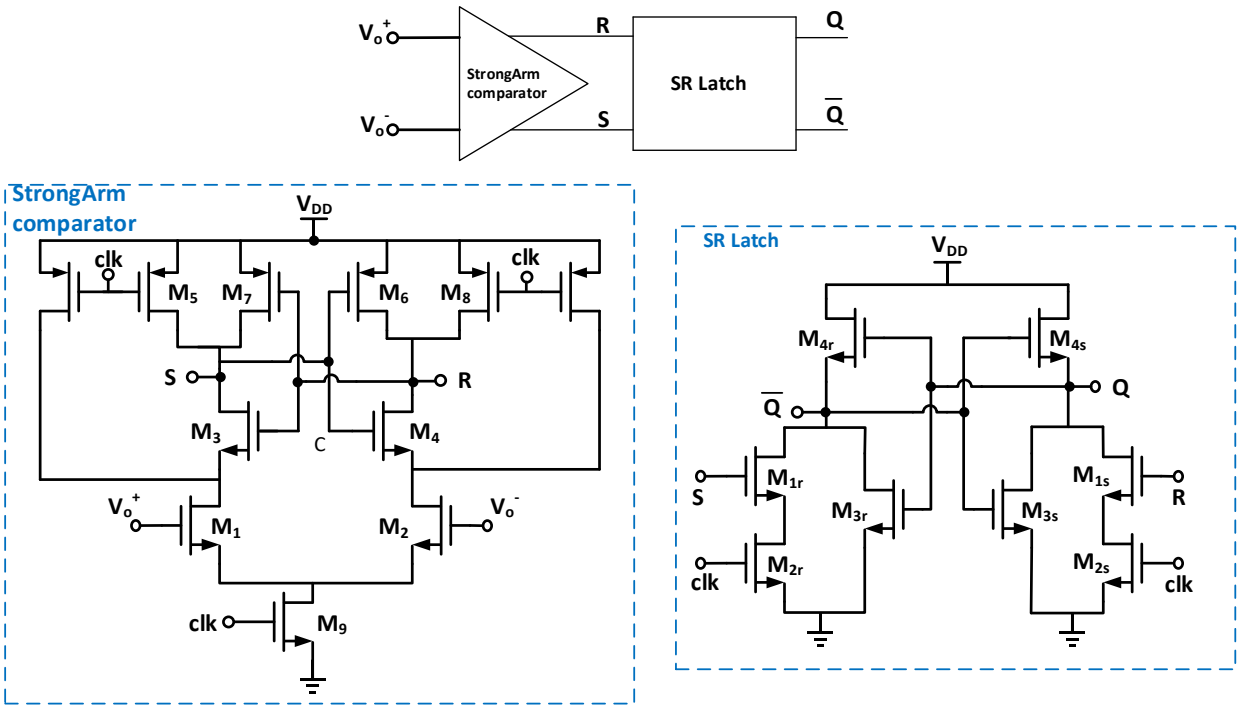

Fig. 6. Schematic of the quantizer block (StrongArm comparator and SR-latch).

Fig. 7. Saturation detection block structure using a 7-bit counter.

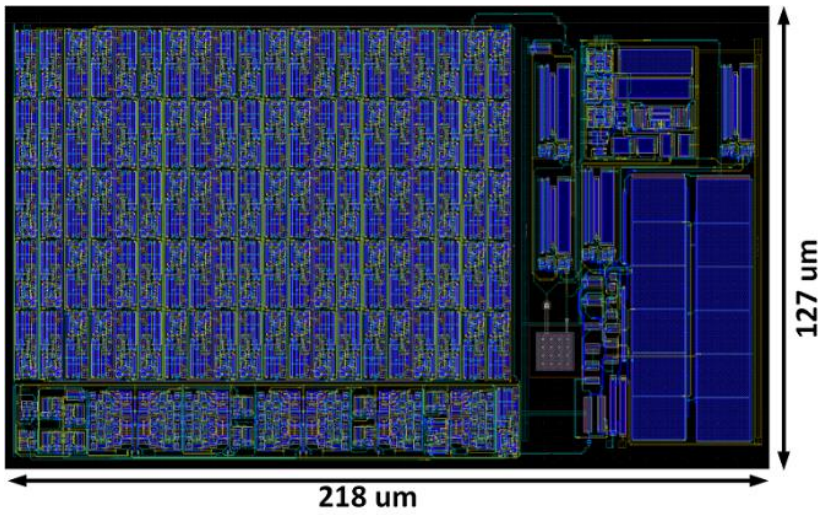

Fig. 8. The layout of the Neural Recording Front-End Circuit (1 channel).

3.4. Step3: Sharing the digital part of the system in different channels

Changing the structure of how to detect the existence of artifacts in the previous part caused a 20% decrease in the occupied area, but still, the presence of 100 registers to approximate and store the artifact domain has a direct effect on increasing the occupied area. The suggested idea to reduce the effect of this part is to share the digital parts of the system, including artifact detection and approximation and storage of the artifact domain between different channels recording neural signals. To improve system performance, we use two active paths in all

channels so that the channel has reached the necessary stability before selecting the main channel at the output. In this article, the system has been implemented to evaluate the system's performance, assuming 32 input channels. On the input side of the sharing digital part, we use two 1to16 Multiplexers (in the same way, on the output side of the sharing digital part, we use two 16to1 DeMultiplexers) along with two general digital blocks, which means two channels are working in full mode at any moment. Using two active channels means that when the channel changes in the presence of the artifact, there is no need to rebuild the channel, and it acts as a system that does not deny sharing.

Fig. 9 shows the Implementation of the neural recorder front-end with digital block sharing and the schedule of each of the multiplexers. For 32 channels, the proposal of digital block sharing makes it possible to use only 200reg+2 Multiplexer(16to1)+2 DeMultiplexer(1to16) instead of using 3200 registers, which occupies an area of 0.013mm^2 per channel, which is about 54% Occupied space is reduced. The placement of the implemented circuit is shown in Fig. 10, and its occupied space is 0.405mm^2 for 32 Channels.

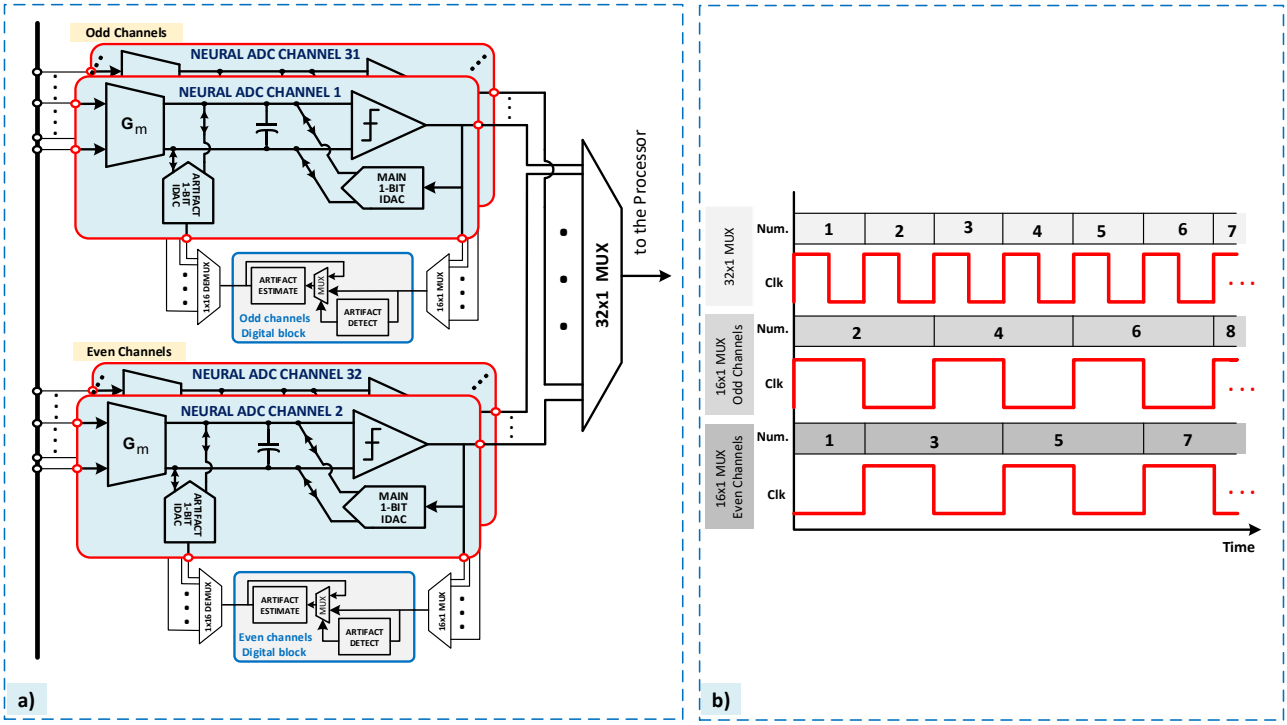

Fig. 9. The neural recording front-end. a) Implementation with digital block sharing, b) The schedule of each of the multiplexers.

4. Circuit simulation results and comparison

The simulation of this system has been done in TSMC180nm CMOS technology with OSR=100, f_s=1MHz and C_{int}=0.2 pF. In this design, the total power consumption is 4.6uW per 1.8V voltage source. The resulting FFT spectrum obtained from 2^{14} points of the CT-DSM output is artifact-free by applying a differential sinusoidal input with an amplitude of 1mVpp and a frequency of 1.465kHz is shown in Fig. 11. The SNDR value for the input with 1mVpp amplitude equals 46dB, and the SFDR value equals 45.8 dBfc. Fig. 12 shows the DR diagram of the system without artifacts. The value of the DR is equal to 45.3dB, which means that the system works for 7uVpp to 1.3mVpp input.

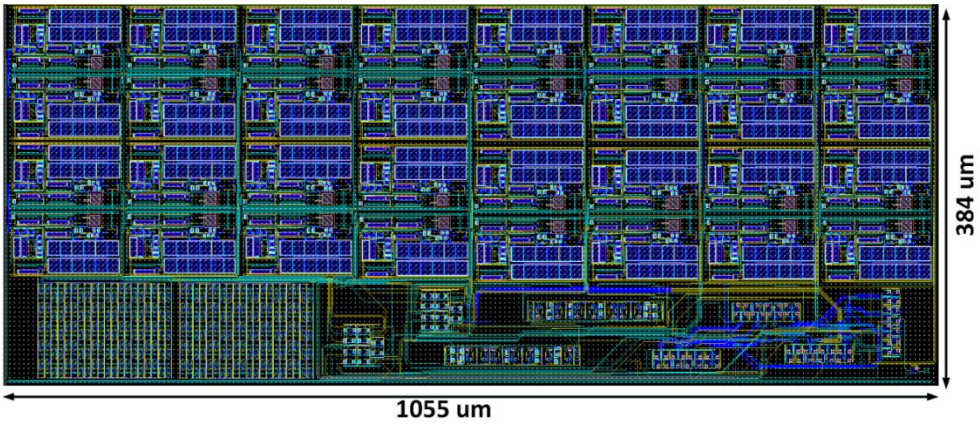

Fig. 10. The layout of the 32-Channel Neural Recording Circuit (with Digital block sharing).

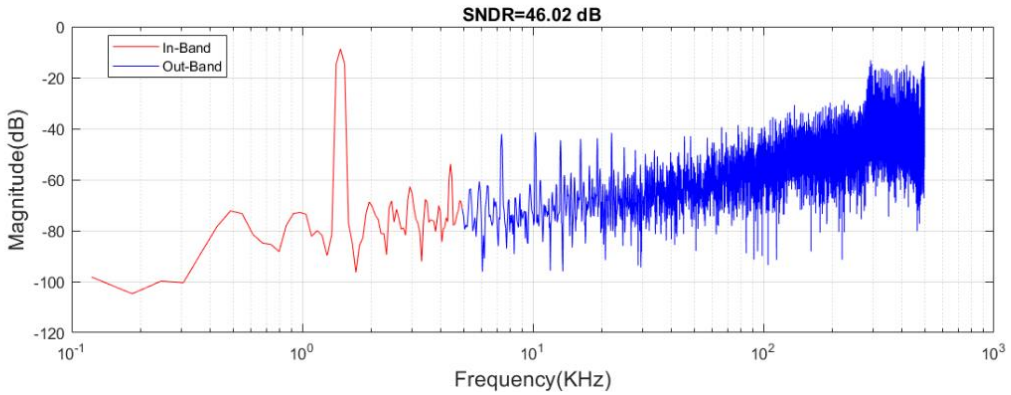

Fig. 11. Output power spectrum density for the implemented Neural Recording Circuit (transistor level simulation).

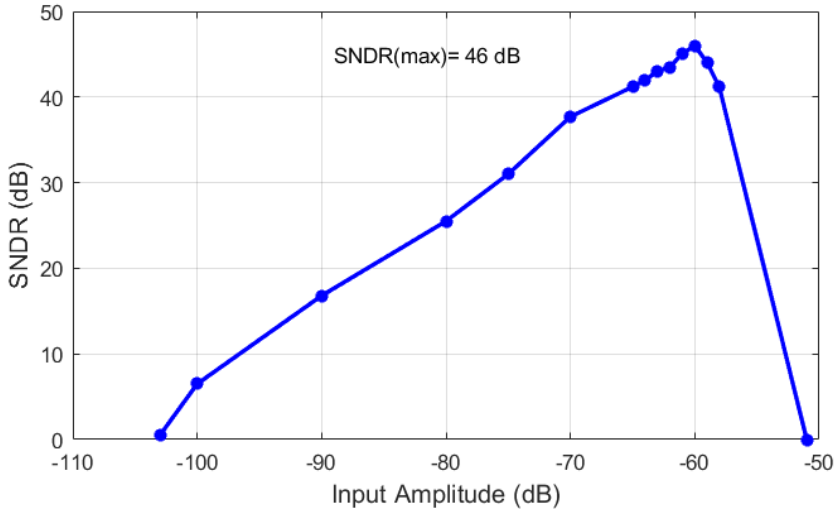

Fig. 12. Simulation results in SNDR over different input amplitudes whitout artifact recovery.

The results of simulating the IRN are shown in Fig. 13. The integrated IRN equals 1.35uVrms terms for the 1-500Hz frequency range. As shown in Fig. 14 show an impedance greater than 200-GΩ for the DC-5kHz range when the chopper switches are on. Fig. 15 shows an example of the transient results for the channel in response to large artifacts. The input DC level changes from 0.9 V to 1.01 V and then to 0.9 V, and the output of the system at the time of saturation detection and estimation of the artifact range is specified. Additionally, to evaluate the maximum tolerable differential artifact for the presented circuit, a 1 mV, 1.465 kHz sinusoid with different offsets from 0 to 145 mV is applied to the channel, and the output SNDR is calculated separately for each case. As shown in Fig. 16, the channel can record up to 135 mV in the presence of differential artifacts while producing an SNR above 40 dB. As a result, the effective input DR value is 45.3+40.3 dB (i.e. (135mV/1.3mV) will be (1.3mV/7uV)).

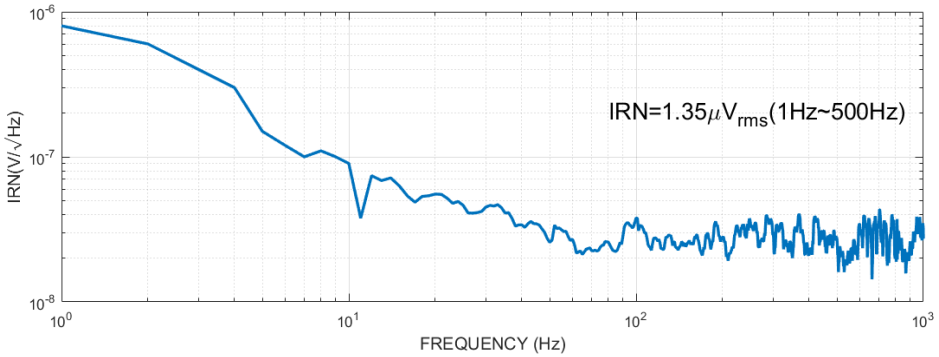

Fig. 13. Density of In-Band IRN in Neural Recording Circuit Simulation Results.

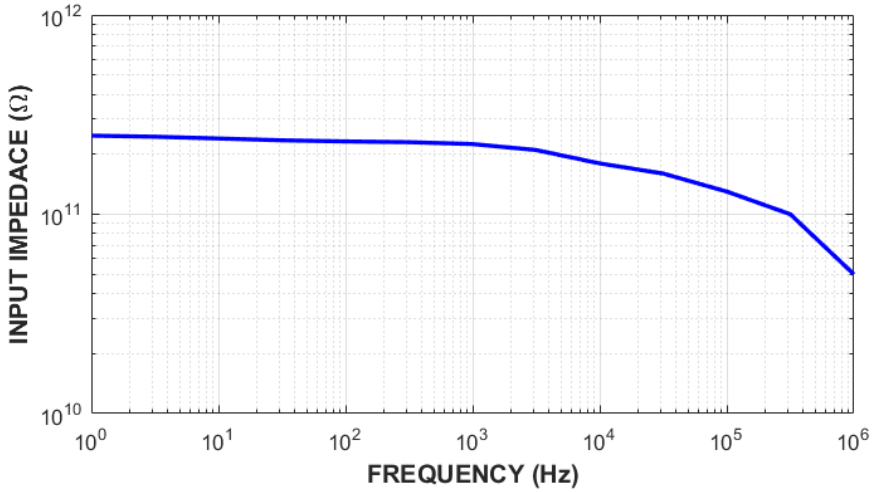

Fig. 14. simulation results for the input impedance of Neural Recording Circuit.

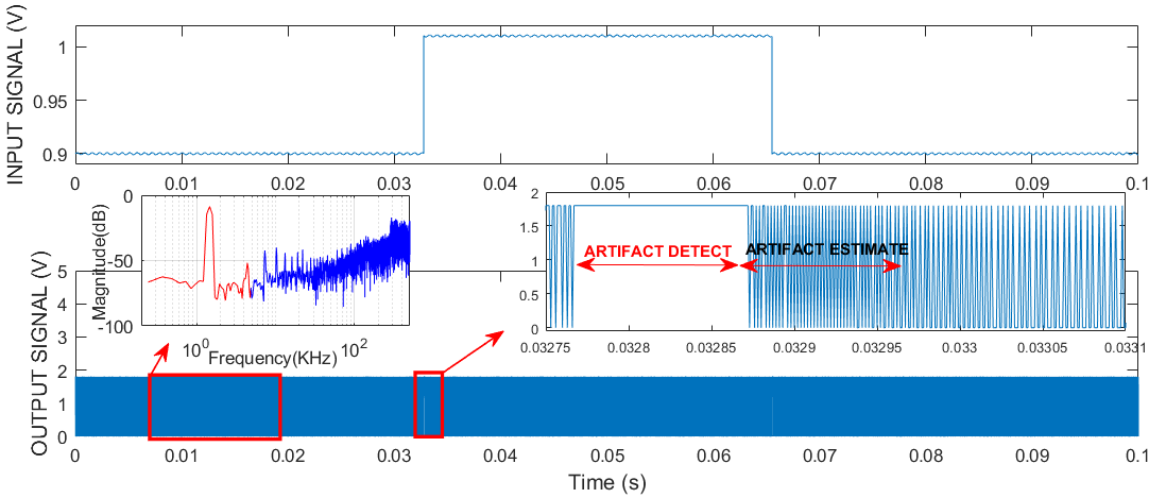

Fig. 15. Transistor-Level simulation results show an example transient response of the presented recording circuit to large DC changes at the input.

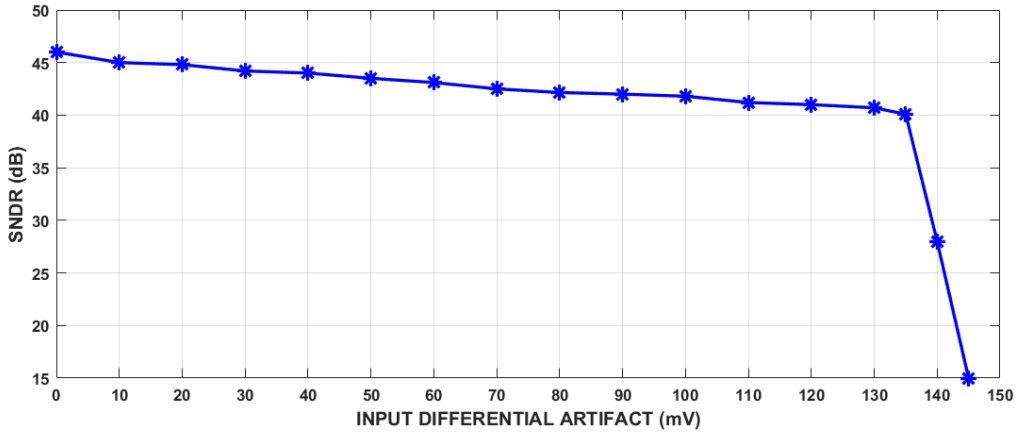

Fig. 16. Simulation results of output SNDR in the presence of various DM artifact magnitudes.

Comparing the state-of-the-art designs in Table II with our proposed method, according to the obtained results, the final goal of the article, i.e. reducing the occupied area and power consumption, has been well achieved, and with digital block sharing, the amount of work done in terms of the occupied area is the lowest.

5. Conclusion

Using an ADC with medium accuracy and low power consumption and removing the artifact range at the system's input can be a good idea for recording neural signals. A 1st-order CT-DSM that performs typical mode conversion of neural signals is used along with a secondary feedback loop for saturation detection and artifact amplitude estimation. In this article, the design and simulation of a forehead block recording 32-channel neural signals has been done. To achieve lower power consumption and occupied area, in this research three ideas have been used: designing a low-power input Gm

block, using a 7-bit saturation detection counter, and sharing the digital part between 32 channels. A 32-channel neural signal recorder was designed and implemented in 180nm TSMC CMOS technology with a bandwidth of 5kHz, and the occupied area per channel was 0.013mm^2. The power consumption of each channel was equal to 4.6uW for DR equal to 45.3+40.3 dB. An integrated IRN equal to 1.27 uVrms was obtained for a 1-500 Hz frequency range and an input impedance greater than 200 GΩ.

Table II. Characteristic summary and comparisons with the state of the art.

Ref.	[4]	[30]	[31]	[20]	[32]	[23]	[33]	[22]	[21][a]	This work[b]
Tech.	180nm	55nm	40nm	180nm	130nm	180nm	180nm	180nm	180nm	180nm
VDD (V)	1.8	1.2	0.8/0.6	1.8/1.2	1.2/0.6	1	1.5	1.8	1.8	1.8
Power (uW)	14.62	48.13	4.68	18.9	1.7	4.53	1.48	4.5	5.4	4.6
Area/Ch (mm^2)	0.0046	0.24	0.025	0.1188	0.023	0.129	0.09	N/R	0.035	0.013[c] /0.028[d]
Bandwidth(kHz)	10	10	10	10	0.5	5.7	1	5	5	5
IRN (uVrms) BW(Hz)	2.51 0.5-1k	12.94	3.6	6.38 0.5-1k	1.6	3.83	1.8 (1-1k)	1.2 (1-500)	1.22 (1-500)	1.27 (1-500)
Max DM Artifact (mV)	-	200	400	102	>200	N/R	57	350	280	270
ZIN Freq.(Hz)	N/R	N/R	N/R	2.7M N/R	1.47 @DC	N/R	2.2G @DC	2G @1k	200G @5k	200G @5k
Effective DR (dB)	57	99.3	91	77	92	66	35	52+40	50+40.9	45.3+40.3
Artifact Recovery Delay (us)	-	<30	-	<10	<1000	N/R	500	20	<200	<200

[a]: Post-layout simulation. [b]: Transistor-level simulation. [c]: with Digital block sharing [d]: with-out Digital block sharing
N/R: Not reported

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